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"Power-Aware Full Adder Design Using Hybrid CMOS Logic with 16-Transistor Architecture"

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***Abstract*— This paper presents a unique hybrid-CMOS 1-bit Full Adder that uses XNOR-XNOR logic and is energy efficient. While the revolutionary full swing XNOR logic is accomplished with five transistors, the suggested complete adder is developed using sixteen transistors. Cadence Virtuoso is used to design the suggested hybrid full adder, while Spectre simulator is used for simulation at a 45nm technology node and 0.8V power supply. The suggested work and recently published work based on several hybrid design styles have been compared. For the suggested hybrid full adder, the propagation delay, power dissipation, and energy consumption are 207.2 pS, 45.32 nW, and 9.39 aJ, respectively. In addition, the impact of temperature and process variations has been examined**.

***Keywords:-* Low power dissipation (LPD), Propagation Delay, energy efficiency, noise margin, Hybrid-CMOS Full Adder (HFA).**

I. INTRODUCTION

In several digital circuits and designs, full adders represent a fundamental logical element. They perform the arithmetic functions in Arithmetic Logic Units (ALUs) that are used in the designs of microprocessors and digital signal processors [1-2], Wallace–Dadda tree multipliers [4-5], and ripple carry adders (RCA) in computer arithmetic [3]. For such high-performance digital applications, high-performance full adders are necessary. For example, in applications with RCAs, the carry-output which is a significant output from the carry-input must be produced within the shortest time possible.

Over the past few years, researchers and designers have been paying more attention to small device structures with high speed and low power dissipation (LPD). All of them are a consequence of the increasing demand for mobile electronics like mobile phones, portable laptops, smart watches, smart calculators, etc [6–8]. However, because of the trade-off between these performance requirements, it is almost impossible for designers to come up with an LPD that has increased speed and smaller dimensions [9–10]. In addition, due to the short channel effects and down scaling, deep-sub micron technology (goes below 100 nm) is also important [11].

In order to satisfy consumer demand of portable electronics and to achieve the most out of the performance, the hybrid-CMOS Full Adder (HFA) makes use of different design styles. HFAs in addition to static CMOS are constructed using different logic types that include pass transistor logic (PTL) [12], complementary PTL (CPL) [13], differential cascode voltage switch (DCVS) [14], double PTL (DPL) [15], swing restored CPL (SR-CPL) [16], and other hybrid design styles such as [17-24, 27-29]. Later on, Section II continues with the review of previously reported full adders and the trade-offs that they are subjected to.

This paper demonstrates an energy efficient scheme of the XNOR-XNOR logic bias is hybrid CMOS 1-bi t Full Adder. In the proposed XNOR logic, five transistors are used. The implementation of the full swing XNOR in the proposed HFA guarantees large noise margin. The remainder of the paper is divided into many sections. The reported efforts are followed by the link of their limitations in Section II. The complete view on the novel structure of XNOR-based HFA which is developed in this work is presented in Section III. The simulation environment and results, as well as discussion, are included in the topics of Section IV. This is done in order and as a requirement, in Section V of the paper.

II. REVIEW OF THE CMOS FULL ADDERS

A full adder's outputs are expressed in the min term as Cout(A, B, C) = ṃ(3, 5, 6, 7) and Sum(A, B, C) = ṃ(1, 2, 4, 7). where the inputs are A, B, and C, and the outputs are Sum and Cout. Many design styles are chosen for either high speed or LPD to implement this. Static-CMOS (traditional), Charge Steering method (CST) [7], Dynamic CMOS [10], CPL, SR-CPL, transmission gate adder (TGA) [21], transmission function Full Adder (TFA) [20], domino CMOS [25], and so on are some of them.

A. Conventional designing of full adder

Static-CMOS design is the conventional method for designing digital CMOS devices. Due to the low mobility of the pull-up PMOS network, proper device sizing is required. The static-CMOS full adders also have a high input capacitance. The pre-charge stage and charge sharing are the dominant constraints in dynamic-CMOS and domino logic. It is easy to achieve high speed and LPD in CST, but the large capacitors used require a large chip size.

Although the optimal chip area may be achieved in CPL, performance is degraded by low swing and poor noise margin. Therefore, the weak PMOS swing restoration transistor is used in SR-CPL to recover the swing.

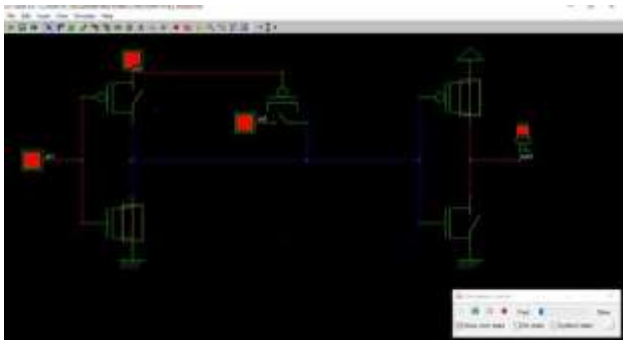

Fig 1: CMOS 5T Full Adder.

To eliminate the intrinsic threshold drop issue, TFA and TGA are also used in the design of the complete adders at the location of CPL.

B. Modules based Full Adder or Hybrid Full Adder(HFA).

The hybrid design style was selected by the author since it provides more freedom and helps to overcome the limits of the conventional design style associated with each of them. Since there are several ways to write the Sum and Cout expressions in equations (1) and (2), the five possible classifications were addressed in [26] by using three modules: module A, module B, and module C. Fig. 1 illustrates the general module classification in HFA logic.

$$\text{Sum} = A \oplus B \oplus C. \quad \ldots(1)$$

$$\text{C out} = A.B + C.(A \oplus B). \quad \ldots(2)$$

The five module classifications are Centralized HFA Module (H as a Select Line), Centralized HFA Module (C as a Select Line), XOR-Static CMOS Based HFA Module, XOR-XOR Based HFA Module, and XNOR-XNOR Based FA Module, as explained in [26]. Depending upon the benefits and uses, each module might be created using a different logic design style.

The balanced XOR and XNOR function in the HFA[27] is implemented using CPL for module A, which leads to minimal noise margin and threshold drop. Here, it is also seen that the outputs of module A are badly produced for a low power source. Although HFA overcomes this low power supply constraint [16], the speed of HFA is affected by the worst-case delay associated with LPD. The energy-efficient HFA[22] has proposed a design that employs modified NAND and NOR logic gates. Other HFAs in [27–30] have addressed LPD but these designs suffer from poor noise margin.

III. PROPOSED HYBRID CMOS FULL ADDER

The following logical equation forms the outputs of the HFA in the XNOR-XNOR-based HFA architecture.

$$\text{Sum} = ((A \oplus B)' \oplus C)' = (X \oplus C)'. \quad \cdots(3)$$

$$\text{C out} = A.X + C.(X)'. \quad \ldots..(4)$$

where the output of XNOR logic is $X = (A \oplus B)'$.

Modules "A" and "B" are designed using XNOR gates, whereas Module "C" is implemented with a 2:1 multiplexer, as the following logical expression dictates. This group acts as the basis for module implementation in HFA in [19]. There are various means through which XNOR functions can be realized in module "A." One method utilizes an inverter to make XNOR after obtaining XOR. Fig. 2 shows the proposed logic implementation for XNOR.

All NMOS transistors have their bulk terminals connected to ground (GND), while all PMOS transistors have their bulk terminals connected to the highest power supply (VDD). It has been noted that in this case, the "P" acts like an XOR function, but for AB=10, it suffers from low swing. This is because transistor M3, being controlled by B (logic "0"), transfers A (logic "1") to node P and so P goes high.

However, M1 is also on and trying to drive node P low with logic "0." Node P settles at VDD−|VTHp| due to transistor M3 being a poor PMOS transistor. Moreover, the swing of HFA outputs reduces by either 2|VTHp| or |VTHp|+VTHn. The above swing is restored by the XNOR logic which uses a static-CMOS inverter to create the output X from the complement of P. Fig. 2(b) depicts the behavior of the proposed XNOR logic as mentioned above. The proposed XNOR realization provides full swing, and hence it is well suited to increase the noise margin of the HFA.

Figure 3 shows the proposed HFA (16T) with a distinctive XNOR circuit and XNOR-XNOR based logic. Modules A and B here describe the full swing XNOR logic designed in Fig. 2(a). VDD and GND are connected to the bulk terminal of each PMOS and NMOS transistor. The 2:1 multiplexer, Module C, employs the XNOR (X) output as a select line.

A transmission gate is added into the 2:1 multiplexer architecture. Here, input C is transmitted at output if X is logic "0", while A is transmitted at output when X is logic "1". From critical path one may observe proposed HFA's worst delay. Here for this architecture, either A to outputs is the critical path.

For testing and verification, the proposed HFA is applied to design a 4-bit binary adder, as shown in Fig. 4. The block diagram of the 4-bit binary adder shows the critical path either from A1 to C4 or from B1 to C4, and each HFA block is designed based on the proposed HFA.

CMOS circuits are usually the components of digital integrated circuits. Now-a-days, the need for power is a basic problem in VLSI architecture. This is due to CMOS

circuits functioning the same amount of time as the other small circuits.

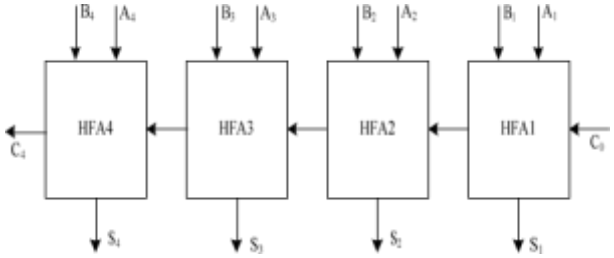

Fig:2 4-bit Hybrid Full Adder.

It gives a sum and two carry bits as output while the 4-bit adder performs the 4-bit addition operation. To boost the performance of the entire system, hybrid full adders use many logic styles within its architecture. The primary motive of hybrid logic style in reducing the number of transistors and power dissipating nodes in the adder cell. A Hybrid adder is an instance of hybrid pass logic using static CMOS, popularly known as HPSC.

IV. SIMULATION RESULTS AND DISCUSSION

Fig. shows the proposed HFA's simulated transient waveform at VDD=0.8V. Here, the LSB is the input C and MSB is the input A. All the inputs range between 0V and 0.8V. The whole output swing is generated for all the logical cases ranging from 000 to 111.

The transistors of the proposed design are designed for high speed with the minimal use of energy. Cadence Virtuoso is utilized for the design of proposed HFA and the simulation was performed in the Spectre simulator using 45 nm technology node at 0.8 V of power supply. The load capacitors were considered to be 5fF while simulating the transients. To validate the effect of power supply variation, VDD is varying between 0.6V and 1.2V. With the help of DC simulations and considering the worst case scenario, noise margin is obtained. In this case, only one input is DC swiped from 0V to VDD whereas the remaining inputs are set at either 0V or VDD.

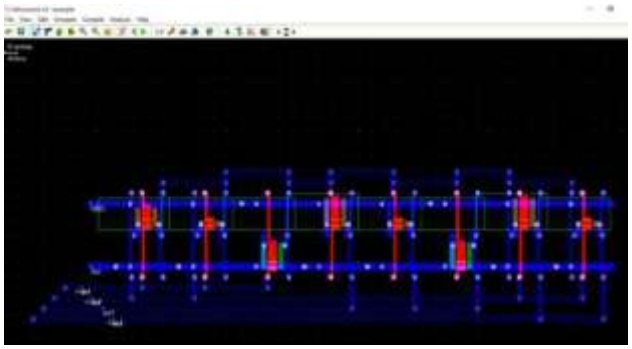

Fig:3 Layout of CMOS Full Adder.

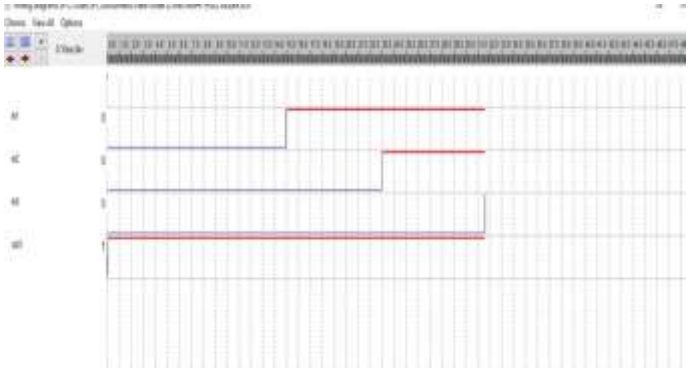

FIG:4 TRANSISTENT WAVEFORM

FIG. PLOTS THE PERFORMANCE COMPARISON OF HFAS IN TERMS OF VDD: (A) PROPAGATION DELAY (B) AVERAGE POWER DISSIPATION (C) ENERGY CONSUMPTION (D) NOISE MARGIN. HERE, FOR COMPARISON, HFAS IN [11, 16, 21, 22, 23, 27, 28] ARE CHOSEN AND ALL THE HFAS HAVE BEEN SIMULATED IN A SIMILAR SIMULATION ENVIRONMENT SO THAT A FAIR COMPARISON CAN BE MADE.

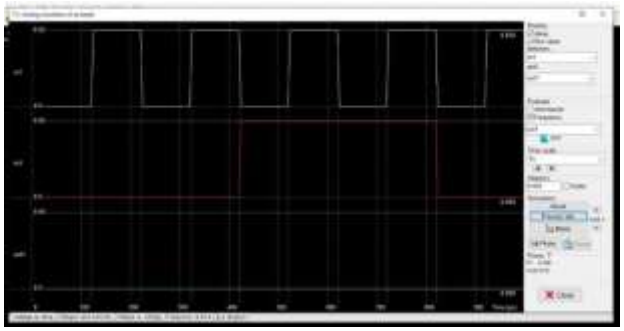

Fig:5 Simulated Transistent Waveform.

Fig. demonstrates how temperature variations influence the proposed HFAs' performance at VDD=0.8V. Here, temperature variations from -200C to 1000C have been considered. As voltage and temperature are linearly correlated, it is observed that power dissipation increases with temperature. Since drain current is linearly dependent on mobility and mobility changes, the delay decreases from -200C to 00C before it starts to increase from 100C onwards.

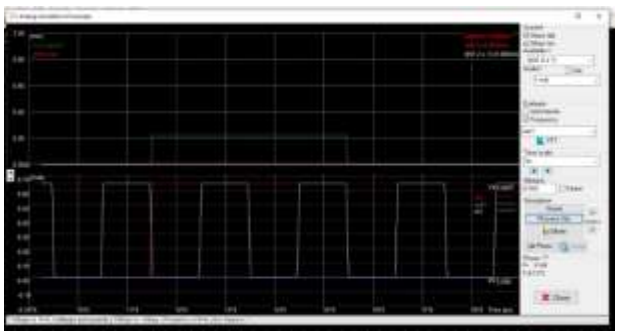

Fig: 6 Simulated Voltage vs Current waveform.

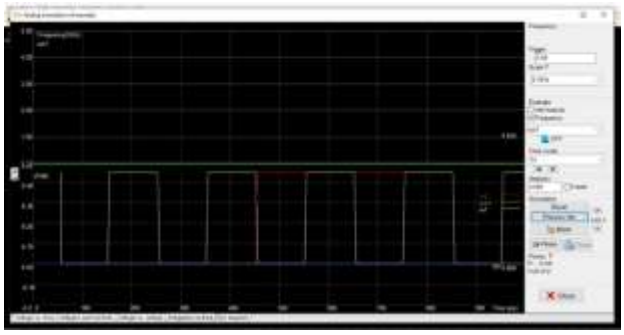

Fig:7 Simulated Frequency vs Time waveform.

Represents the performance overview of the proposed 1-bit HFA at all the process corners. There are five possible process corners: normal or typical (TT), fast-fast (FF), fast-slow (FS), slow-fast (SF), and slow-slow (SS). It has been noted that the FF corner has the minimum delay as well as the maximum power dissipation, while the SS corner has the highest delay and the largest power dissipation. Process corner variation has less of an effect on the noise margin.

Fig:8 Eye Diagram.

Lastly, the suggested work has the least power consumption at 0.8V of VDD and the largest noise margin compared to recently published works according to the performance comparison of the suggested HFA that has been described in Table all VDD. The III. Here, it has been observed that the suggested HFA has extremely high noise immunity and uses the minimum amount of energy in terms of power dissipation and propagation latency.

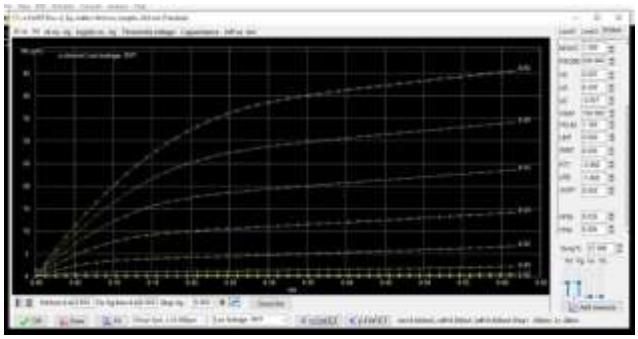

Fig:9 Drain Current vs Drain Voltage.

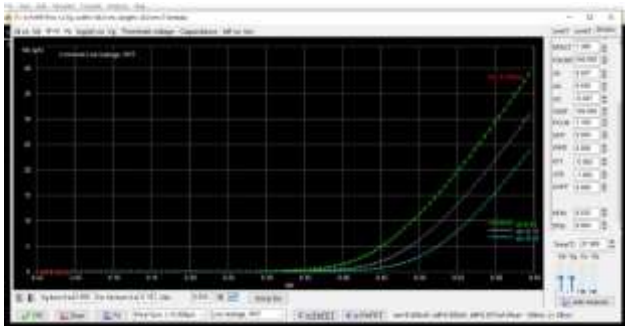

Fig:10 Drain Current vs Voltage Gain.

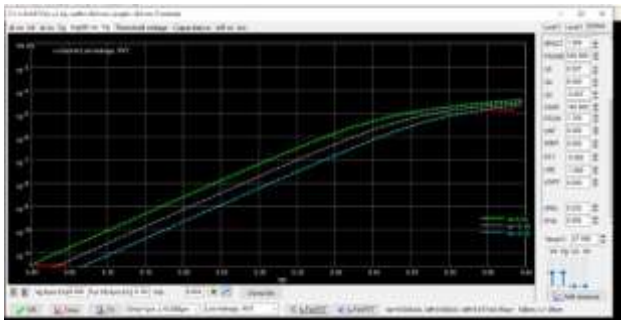

Fig:11 log(Id) vs Voltage gate.

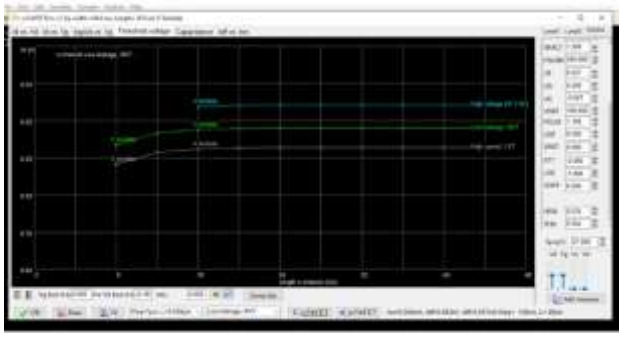

Fig:12 Threshold Voltage.

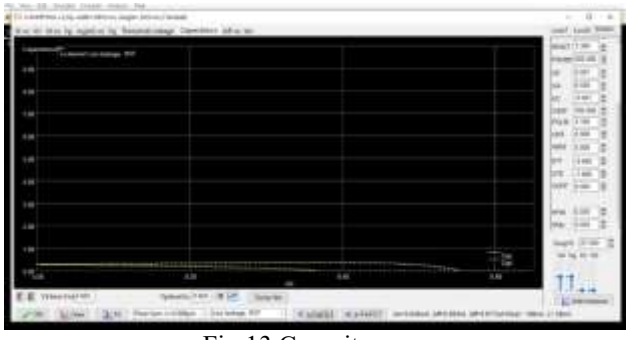

Fig:13 Capacitances.

V. CONCLUSION

This research introduced a fresh HFA architecture based on an XNOR-XNOR module where five transistors fully implement XNOR logic. The HFA suggested in this paper delivers the maximum noise margin, as well as minimum energy consumption. Cadence Virtuoso tools are utilized for simulating and comparing 1-bit proposed HFA circuits employing 45nm CMOS technology with VDD=0.8V. In this scenario, the energy consumption, the power dissipation, as well as the propagation delay values are,

respectively, 9.39aJ, 45.32nW, and 207.2pS. This design has also resulted in a reasonable noise margin. According to similar simulation environments, a comparison of seven HFAs with the proposed HFA has been published. Compared to the HFA[21], HFA[23], and HFA[27], the proposed HFA is 11%, 23%, and 44.8% energy efficient, respectively.

Only 16 transistors are required to design the proposed HFA, therefore a relatively small chip area is required. Even though discussion and performance improvement have been done, it has been observed that the module A of the proposed HFA is asymmetric, which is why the logic "0" danger peak affects the performance. Then, a 4-bit binary adder is designed using the proposed HFA. Based on the critical route at 0.8V of VDD, the worst-case delay in this scenario is 551pS.

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