RB Journal of Lib & Information Science
(UGC Care Group I Listed Journal)
ISSN: 0972-2750
Vol-12 Issue-12 No.03 2022

High-Performance PMOS Sense Amplifier with Reduced Power Consumption

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Abstract— **Memory circuits are found to be critical in enhancing the performance, functionality, and reliability of sense amplifiers. In this paper, two novel circuit designs have been proposed to mitigate the shortcomings of conventional designs. One of them is the PMOS-biased sense amplifier that has an outstandingly high output impedance. This design reduces sense delay and power dissipation to a substantial extent with no loss of functionality compared to traditional sense amplifiers. This design reduces power consumption and delay, providing an efficient alternative for conventional sense amplifier circuits which do not compromise performance. Efficacy and overall performance were simulated and analyzed for the proposed sense amplifier designs in view of their latent potential for improved memory circuit efficiency.**

Keywords — Sense amplifiers, Memory circuits, PMOS-biased sense amplifier, High output impedance, Sense delay reduction, Power dissipation, Circuit performance, Conventional designs, Simulation and analysis, Memory circuit efficiency.

I. Introduction

In digital logic design, memory blocks play a crucial part in various systems, including digital signal processors (DSPs), microprocessors, microcontrollers, and computers. Devices including audio players and digital cameras rely on flash memory to store data in forms such as images, audio, video, and speech. They must have low power consumption yet provide high performance along with considerable storage capacity, all highly integrated into a single chip. Low sensing delay and high memory capacity are what will accomplish the quality and reliability of such data retained in them.

To fulfill this, sense amplifiers are used to amplify the small voltage differences available on bit lines at some well-defined sensing instants. The functionality of the memory system largely depends on the proper timing of the SAE signal. If it asserts the SAE signal sooner than it should, the sense amplifier can often not amplify the small voltage differences correctly, thereby violating data integrity. Conversely, if the SAE signal is deposed too late, it leads to increased access time and more power consumption, thus reducing the efficiency of the system. Therefore, the proper timing of the SAE signal is essential for the efficient operation of high-speed, low-power SRAM cells, resulting in improved memory performance in modern digital applications.

II. PMOS Bias Type Sense Amplifiers

A. Sense Amplifier Circuit-1

The proposed Circuit-1 is a circuit that offers the high impedance output along with eliminating all the static errors, making it a powerful circuit to be used in efficient memory operations. Fig. 1 shows the gate terminals of transistors T1, T2, and T17 short-circuited, which essentially performs the critical function of the circuit. Using this differential mechanism with the current, the proposed Circuit-1 achieves better reliability and accuracy critical for the requirements of low power consumption and minimal sensing delay in modern memory applications.

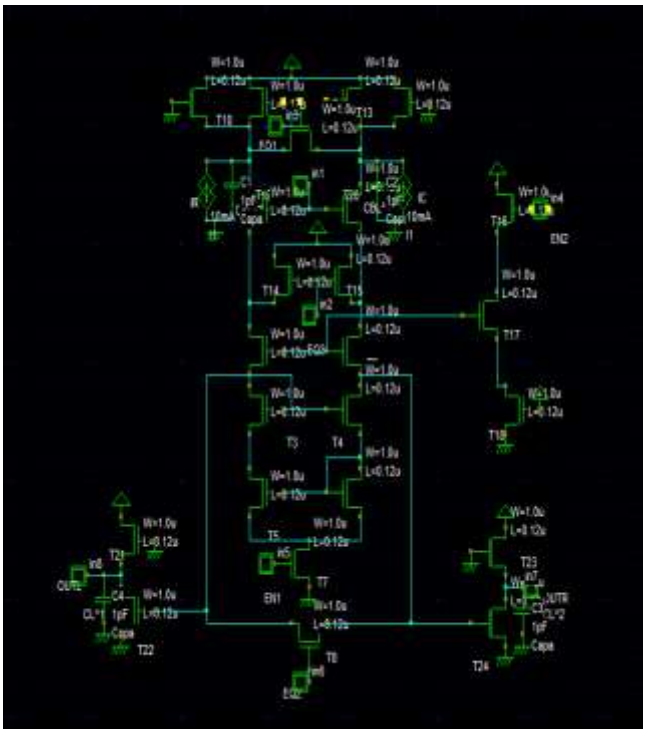

Fig. 1. Proposed sense amplifier circuit-1

In the new layout, the sense amplifier design has transistor pairs T3-T4 and T5-T6 in a symmetrical configuration such that the input and output potentials are nearly identical. Consequently, the input and output currents are nearly equal and distribute correctly. This self-cancelling results in a lower count of transistors compared to designs in the conventional sense amplifier so that it significantly reduces both sense delay and power dissipation.

Traditional PMOS-biased sense amplifier which results in the greater number of transistors and thus results in increased power consumption and complexity. The sense amplifier designed in this work has been shown in Fig. 1. It is apparent that each of the outputs is derived at strategic points: OUTL is taken across transistors T1 and T3, while OUTR is obtained across transistors T2 and T4. The proposed sense amplifier greatly improves on conventional counterparts because it significantly simplifies the circuit without compromising performance for modern low-power, high-speed applications.

B. Sense Amplifier Circuit-2

The second design of the sense amplifier is presented in Fig. 2 with further improvements in terms of power efficiency and speed. In this topology, the output nodes are placed in a way to maximize performance. For instance, the output OUTL is taken across transistors T1 and T5. Similarly, the output OUTR is taken across transistors T2 and T6.

This configuration provides for efficient signal amplification and retains a simple circuit structure. The changes made to this sense amplifier significantly reduce power, minimizing the flow of unnecessary current while maximizing transistor use. The sense delay is also reduced considerably to realize faster access to data and overall performance.

Hence, the second proposed sense amplifier, focusing on reducing the power dissipation and delay challenges, offers a refined and efficient alternative to conventional designs that meet the demands of modern memory applications based on high speed and low power.

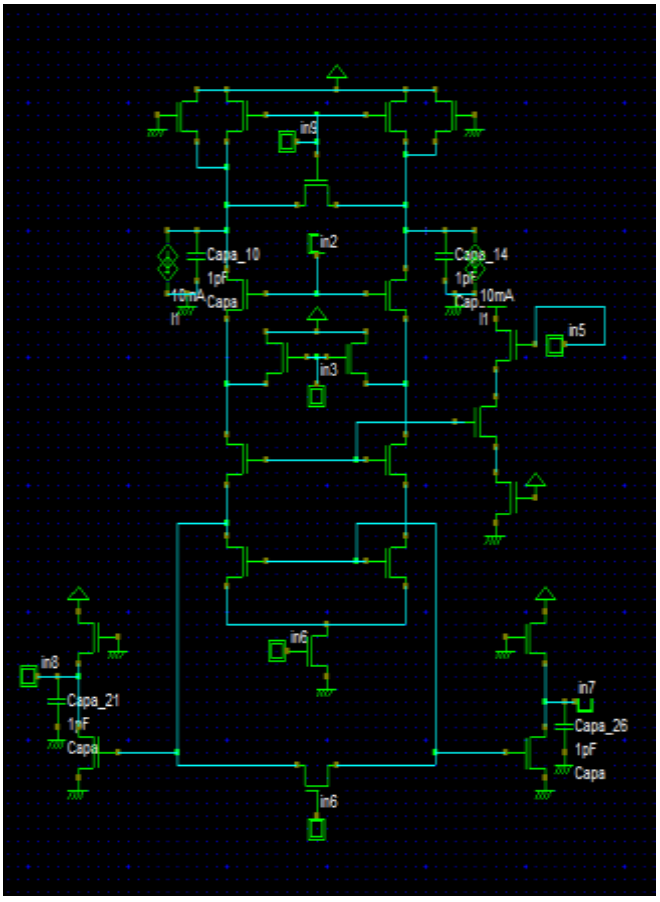

Fig. 2. Proposed sense amplifier circuit-2

III .SIMULATION RESULTS

The simulation of the proposed sense amplifiers was performed. In order to have consistency and accuracy, all the simulations were performed with identical fan-in and fan-out configurations. As can be seen in Fig. 1, in this sense amplifier, a current mirror structure is drawn in where transistors were designed with equal dimensions and a width-to-length (W/L) ratio 0.9µm/0.18µm The reference current Ic and memory current were set at 1µA and 10µA, respectively. Load capacitances of 50fF were applied at the output nodes, while a bit-line capacitance of 1pF was used, reflecting realistic operational conditions.

It is found that the performances of the sense amplifiers were highly dependent on the bit-line capacitances, which directly affect the sensing delay. The transient analysis for the first proposed sense amplifier. This study demonstrated that the sensed delay was reduced as the supplied voltage increased. Such results are indicative of the strength of the design proposed under different supply voltages and thermal situations.

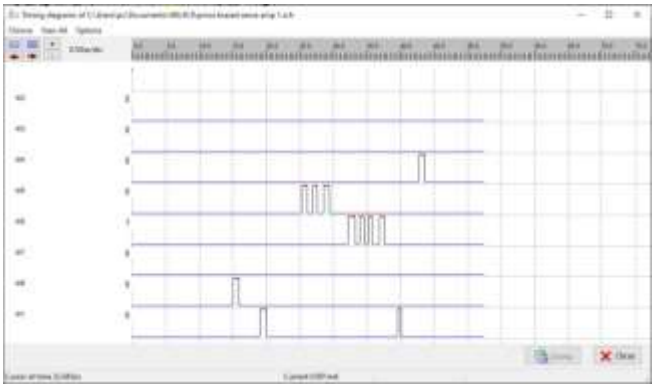

Fig. 3. Transient analysis of proposed circuit-1

Similarly, transient analysis for the second proposed sense amplifier is elaborated and corresponding characteristics of sensing delay versus +VDD. Similar to the first design, the second sense amplifier also shows a decrease in sensing delay as +VDD increases from +1V to +3V. Such a consistent behavior in both designs further indicates their efficiency and adaptability for high-performance memory applications. The results are graphically shown to present clarity in comparison of the sensing delay performance. To give a more extensive view, the results are represented graphically, enabling a direct and clear comparison of the sense amplification delay performance between both designs. The graphical representations thereof clearly delineate the improvements attained and confirm that the sense amplifiers proposed are superior to other conventional schemes. The plotted data also highlights the fact that both schemes maintain optimal performance throughout a large operating supply-voltage range, thereby keeping the versatility for every practical scenario.That the second sense amplifier proposed closely matches the performance characteristics of the first design while preserving its novelty further establishes the validity of the methodology proposed..

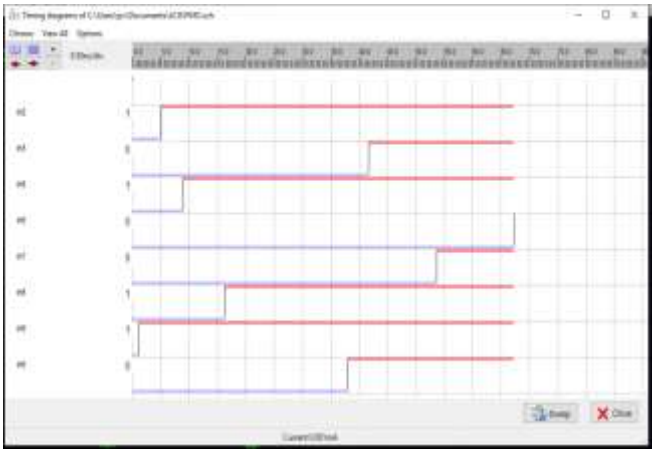

Fig 4. Transient analysis of proposed circuit-2

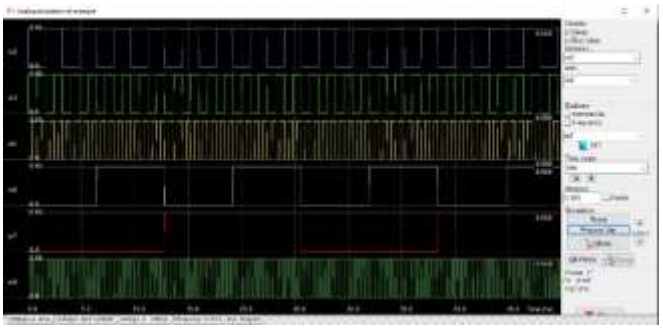

Fig 5. Analog simulation example

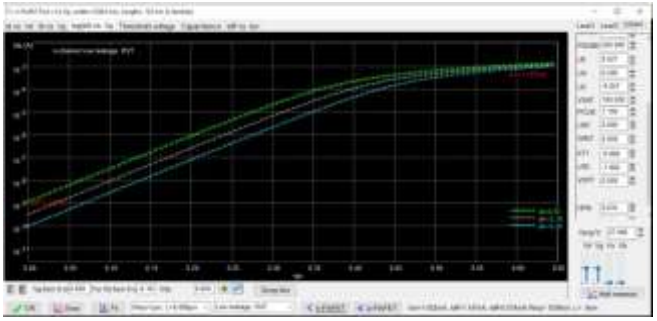

Fig. 6. Sensing delay time Vs different voltages (+VDD)

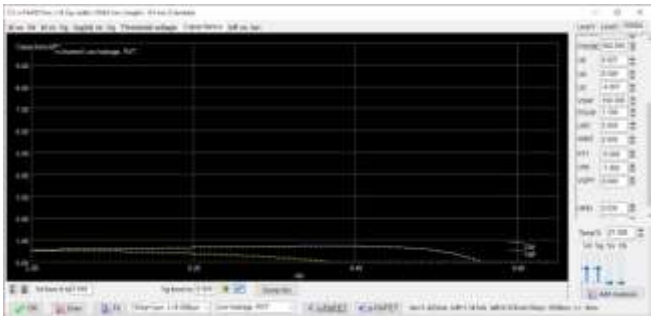

Fig. 7. Sensing delay time Vs different voltages (+Vdd)

IV. Conclusion

Development and analysis of two innovative sense amplifier designs. Transient simulation results of the proposed sense amplifiers were similar to theoretical expectations, therefore validating their performance and design efficacy. Graphs were also produced to show simulated sensing delay, with the supply voltages varied, in an effort to visually represent circuit behavior under different conditions. The proposed sense amplifier designs are transistor-count reduced, thereby greatly minimizing both sensing delay and power dissipation compared to conventional designs. This streamlined architecture increases efficiency, making the circuits suited for modern memory applications that demand high speed with low power consumption. The simulated power dissipation for the proposed designs clearly underscores their energy efficiency. In the first proposed circuit, it was possible to achieve a power dissipation of 80.05nW, whereas the second circuit showed even less power dissipation of 35.9nW. These results point out that the proposed designs are effective at achieving optimal performance with minimal energy usage and thus are novel developments in the technology of sense amplifiers.

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