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Optimized 8-Bit ALU Architecture with Low Power Consumption Using 17T Full Adder

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Abstract-- This paper presents an innovative 17-transistor (17T) full adder design, referred to as the full snake, and its application in developing a high-performance Number Juggling Arithmetic Logic Unit (ALU) architecture. The proposed design significantly reduces the power consumption of digital processors while also minimizing delay, achieving an efficient power-delay product. As a core component of a digital processor, the ALU performs essential arithmetic and logic operations. Enhancing its speed while reducing power usage can lead to improved system throughput. Additionally, the designed 17T full adder generates both Sum and Carry outputs using only multiplexing logic, ensuring compactness and efficiency.

Keywords—ALU, XOR, Multiplexer, Adder, Design, Power, Delay, Processor

Introduction

In the rapidly evolving world of technology, there is a growing need for innovations that minimize power consumption, especially with the increasing reliance on battery-powered devices such as laptops, wearables, and smartphones. This demand has fueled the advancement of low-power VLSI (Very Large-Scale Integration) design, a field where researchers explore semiconductor technologies to optimize the trade-off between propagation delay and power dissipation. A significant area in low-power digital circuit design—particularly in components like microprocessors and ALUs (Arithmetic Logic Units)—is based on Complementary Metal-Oxide-Semiconductor (CMOS) technology. In CMOS devices, the static power consumption is primarily due to leakage currents, while the majority of dynamic power is dissipated due to switching activity, especially when charging and discharging parasitic capacitances within logic gates. To effectively manage power consumption at the device level, techniques such as voltage and frequency scaling, capacitance reduction, and supply voltage optimization are employed. These strategies help reduce overall power usage regardless of the system-level power management policies. The microprocessor, being the core of any digital system, performs billions of operations per second. Its performance heavily depends on the efficiency of its Arithmetic Logic Unit (ALU), which handles all arithmetic and logical computations. Therefore, improving the ALU's design is crucial for enhancing the processor's operational speed and energy efficiency. In this study, we propose a 17-transistor (17T) full adder design, referred to as the full snake, to significantly reduce both power consumption and delay, thereby optimizing the Power-Delay Product (PDP) of the ALU.

II. EXISTINDESIGNAPPROACH

The core components of an Arithmetic Logic Unit (ALU) are the multiplexer and the full adder—referred to in this context as the full snake—which can be optimized in various ways to achieve an ideal design. Numerous studies have explored high-speed and low-power full adder architectures, including Transmission Gate (TG) based full adders [4][5], 11-transistor low-power full adders [10], and Hybrid Full Adders (HFA) [1]. Additionally, FinFET technology has been employed in ALU design, offering improved performance through its dual-gate structure, which significantly reduces leakage currents and enhances circuit efficiency [8]. However, FinFETs are more expensive than traditional planar CMOS devices due to the complexity of fabrication. The use of multiplexers, particularly with gate diffusion input (GDI) techniques, has been previously explored for their area-efficient and power-saving properties [11]. For operations requiring low voltage, the GDI approach remains highly effective and reliable [13]. In this paper, we propose a robust ALU architecture that utilizes NMOS-based multiplexers and a 17-transistor full adder based on pass-transistor logic style [12], resulting in a compact and energy-efficient design.

The proposed 17-transistor (17T) full adder demonstrates exceptional efficiency in terms of delay and drive capability. Compared to the existing 10T full adder designs, the increased speed of operation of the 17T architecture effectively compensates for the additional transistors used [6]. Furthermore, the overall performance of the ALU is significantly improved by incorporating low-power XOR gates, as discussed in previous studies [1].

III. The design proposed

Design by Sharma et al. [2] has shown promising results in terms of delay and power dissipation. However, their architecture demonstrated transient errors in arithmetic outputs for specific input combinations such as "000," "010," and "110." This necessitated the addition of an extra NMOS transistor at the output of the full adder (referred to here as the *full snake*) to stabilize the result. Unfortunately, this modification introduces additional RC delay at the output node, resulting in load-induced degradation—an undesirable effect.

Our proposed 8-bit ALU eliminates the need for such corrections. It uses a 17-transistor full adder (17T full viper) and NMOS multiplexers, which together optimize performance while reducing both area and power-delay product (PDP). The full adder and multiplexer are the most space-consuming components in an ALU layout. Hence, improving their efficiency is crucial.

A major challenge in existing ALU designs is the excessive intra-module interconnects between multiplexers and adders. These internal connections contribute more to delay than inter-module links, as they increase the parasitic capacitance and RC delay, especially when routes overlap. The total capacitance at these interconnects is given by:

During switching events, these interconnects cause a rise in dynamic power consumption due to increased path capacitance. At higher operating frequencies, the power dissipation escalates,

further stressing the circuit.

To address this, our design focuses on minimizing gate count and improving logic efficiency. The 17T full viper offers

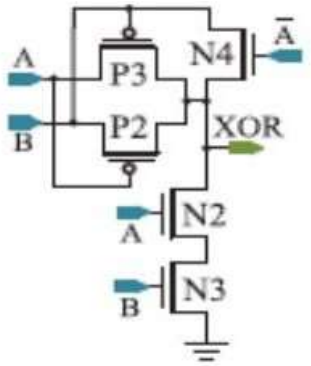

Fig. 1 Low power XOR gate

exceptionally low propagation delay, making it ideal for constructing an 8-bit ALU. Furthermore, the Sum and Carry outputs are generated with nearly identical delays, enabling high-speed performance. The design also integrates low-power

S0	S1	S2	OPERATION
0	0	0	ADDITION
0	0	1	XOR
0	1	0	XNOR
0	1	1	NOT
1	0	0	SUBTRACTION
1	0	1	AND
1	1	0	OR
1	1	1	NOR

XOR gates and efficient multiplexers to enhance overall throughput.

As the ALU is a vital component in digital processors—handling operations such as addition, subtraction, complement, XOR, AND, OR, etc.—we implemented control via a 3-bit selector (S2S1S0). This selector determines the specific operation to be performed, as detailed in Table 1. Depending on the application, a processor may utilize one or more ALUs for parallel processing.

In summary, our 8-bit ALU architecture, based on the 17T full viper, not only improves speed and reduces power but also overcomes issues such as output instability and excessive area consumption. This design is both compact and robust, making it suitable for high-performance, low-power digital systems.

TABLEI.TRUTHTABLE FORALU

Thetwocritical componentsoftheALUthat wareproposing aremultiplexersandadders.Additionally, XORgates areused in the design of the actual adders.multiplexers. Other reason signals, such as AND or perhaps, can be generated using the same XOR and an associated reason style. Each of the components we used for our design are exposed in the followingsubsections,followedbytheproposed8-cycleALU.

A. LowpowerXORgate

Our 17T complete snake configuration employs a low power XOR door [1]. There are five semiconductors in the gave XOR. Further, the circuit's basic way is with nearly no NOT doors. Later, in contrast with regular entryways, this perfect door allows brief pause and prevalent drivingcapacities. Besides, as observedinFig. 1, there are topsy-turvy capacitances at the bits of feedbacksAnandBoftheXORcircuit.Additionally,the bitsoffeedbacksAnandBofsemiconductorsN2andN3 donothaveidenticalcapacitancesunderidealconditions. Later, thesemiconductor with a low input capacitance is connected to the info A, which is also connected to the CMOS inverter. The circuit's power requirements are

B. NMOS-Multiplexer

In an ALU, multiplexers play an important role in transferring between different operations. We are adopting the NMOS pass semiconductor rationale approach, which is placed in our design. multiplexers plan. It uses four semiconductors. Therearetwoof them andbothof themareNMOSsemiconductors responsible for selection of information signals. Limit voltage for both NMOS semiconductors are identical. Besides, their length, expansiveness and other practical parameters are also the same.

Weuse2-to-1 and4-to-1 multiplexers, dependingonthe numberofsourcesofinformationneededandthenumber ofusableselectlines.Therationaleforusingtherationale style based on NMOS forThe multiplexer gives an advantageofadesignhavingmoredirect witha minimal numberoffoursemiconductorsinmostgeneral.Thus, this is decreasing association delay as well as parasitic capacitances. This multiplexer is also showing the smallestdelayintermsofearlangdefercomputation,that is,betweentheinfohubandtheresulthubsthananyother multiplexer.

It shows lesser power consumption and latency because of overlaying attributes. It also performs much better in our design incomparison to manyrationalecircuits such as double pass-semiconductor rationale and CMOS Transmission gateway (TG).

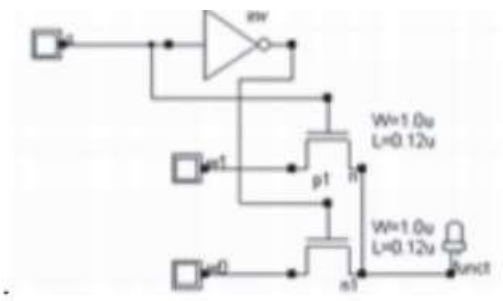

Fig. 2 PTL based 2-to-1 NMOS multiplexer

C. Novel17TFullAdder

OurALU configuration makes use of the FA-17T, or 17 semiconductorfullviper.ThetotalviperusedinourALU configuration is depicted in Fig. 4. Also, the reason for this total Our viper in theALU completes every number juggling activity tabulated in Table 1. Also, as just recently mentioned, low power XOR doors are used for the design of our viper. Also, as mentioned above, we have used a 2-to-1 multiplexer based on NMOS pass semiconductor logic family for our whole viper design.

This viper structure benefits from low power consumption,highactivityspeedforthegenerationofthe Convey and Aggregate signs, and invariance to gadget scaling. In addition, instead of current half and half full- snakedesigns, for example, 17T,19T, 20T,and22T.We found that the proposed 17T complete viper's power necessities have diminished by 71.5%, from 4.08 e-6 W to1.16e-6W.Ontheselines,activityspeedhasincreased by83.8%,meaningtheaveragedelayhasdecreasedfrom 59.10 ps to 9.52 ps, and the delay was found to be29.55 ps.Thisalsooffersaclearerplanlayout.Thepresentation study as discussed above is demonstrated in Fig. 3.

Also, if we compare our 17T full viper with 11T or 10T full adders, then we find that though both full adders appear to provide a less number of semiconductors, the 17T FAprovides a response that is 85% faster to spread thecarrysignal.Also,17Tfulladdersofferareductionof 92% in power usage. The average sleep and power consumptionfor a11Tfullsnakeare64 nsand16 e-6W, respectively.

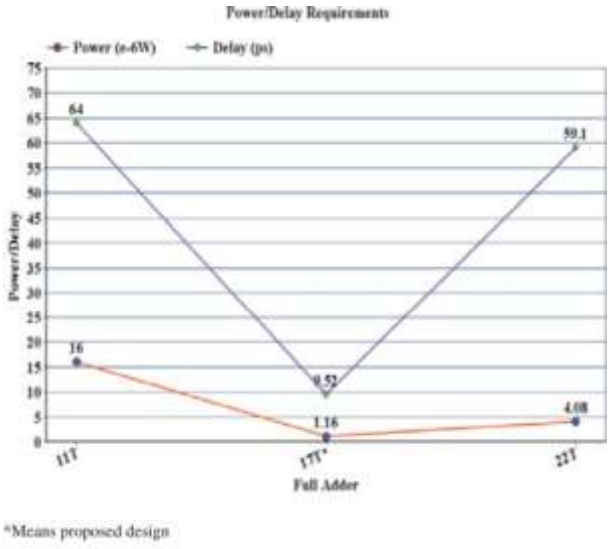

Fig. 3 Power/Delay comparison of the proposed 17T full adder with 11T full adder and 22T hybrid full adder

The justification used by the whole viper says that the Total(Cout)signalequalstheinformationsignalAnorB whenever A XOR B = 0 and equals Convey In (Cin) otherwise signal. Besides, theTotal sign (Total) is equal to the Convey In (Cin) signal whenever A XOR B = 0; otherwise,itisequaltothecomplementoftheConveyIn (˜Cin) signal.

We ought tonotethat we would havebeen ableto easily have cleared the multiplexer's select line using a low powerXNORentryway,whichis,afterallequivalenttoa XOR door. However weareintentionallyusinga CMOS inverter instead ofAXNOR B to add to the midAXOR B signal. In this way, the absolute number of semiconductors neededis drasticallybrought downfrom 25 to 17.

Besides, there is an added advantage to picking the NMOS multiplexer among the few multiplexers that are available, which we address currently in segment B. Besides, we utilize an extra NMOS multiplexer to make the Total sign rather than a second XOR entryway. Because of this, the regular power utilization of the NMOS multiplexer, which is 112.9e-9 W, is lower than that of the XOR entryway, which is 359.0e-9 W, in the event that an extra multiplexer is utilized rather than a XORentryway.Thus,ourvipermakestwounmistakable signs — Total and Cout — by consolidating two comparable multiplexers. Besides, there is virtually no difference in the postponements of proliferation of CompleteandAggregatesigns fromtheir contribution to the result.

D. Proposed8-bitALUDesign

Initial, three specific modules — the NMOS multiplier, XOR gate, and 17T Full Viper — are used to create the proposed 1-bitALU cell. In addition, We present a 8-bit ALUthatcanperformmorearithmeticoperationssuchas subtractionandadditionallogicaloperations suchasNOR

Three choice lines, one carry input/yield per cell, two 8- cycle sources of info, and one 8-bit yield are the constituentpartsofthegiven8-digitALU.Theformation of the proposed ALU follows 45 nm innovation. Low powerXOR[1]andNMOSdoors,associatedwithflowed multiplexers, areusedtoperformthecoherent tasks.The total viper that was used

This ALU unit itself consists of equal XOR gates and multiplexers; therefore, it appears to be a series of XOR entryways that have been filled with the aid of the multiplexers. We need a total of sixteen 4-to-1 NMOS multiplexers, eight 2-to-1NMOSmultiplexers, andeight 17T Full Adders for an 8-digit ALU.

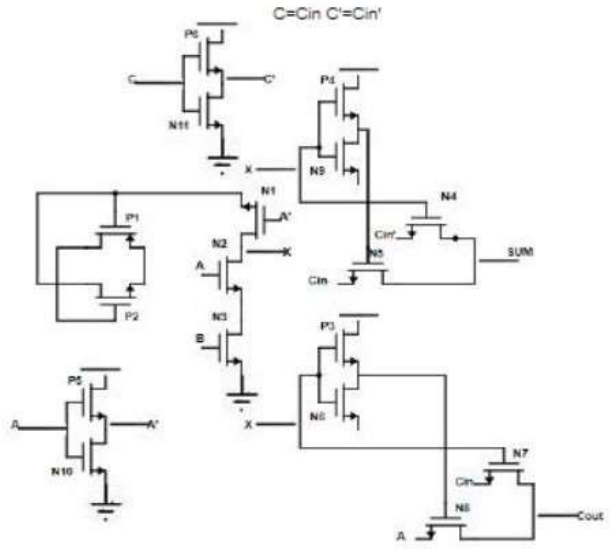

Fig. 4 Proposed 17T full adder

II. SIMULATIONSANDRESULTS

TheRhythmVirtuosoEDAdevicev15.0in45nmprocess innovationwasusedtoassistinthedesignandsimulation. Thereisa layoutoftheOur proposedALUconfiguration makes use of another 17T full snake. With a functional recurrence of 1 GHz, we have made use of a 3-terminal MOSwitha1.2Vpowersupply.TheinfoflagsA,B,and Cin have been designed as beating inputs with rise/fall

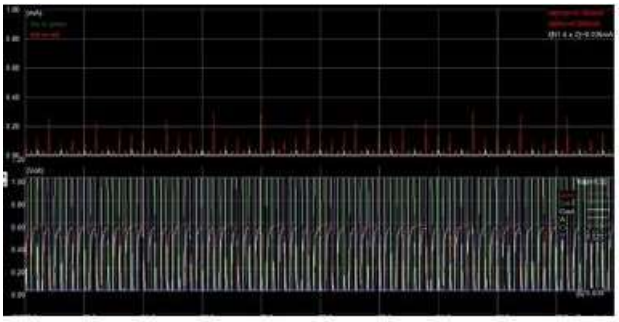

Fig. Propagation delay and power transient of 17T full adder

seasonsof2pseachandseparatetimespansof4ns,8ns, and 16 ns. Furthermore, the recreation consequences of theinventive17T complete viper representing. 6- 8. AND to expand the operations. The schematics of the proposed 1-bitALUcell and the8-cycleALUdesign are shown in Figures 9 and 12, respectively.

Inaddition,therecreationwaveformshowstheAggregate

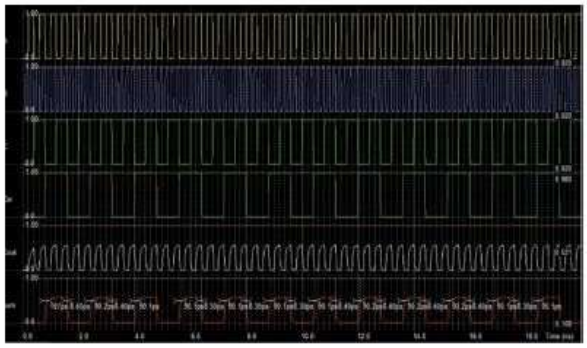

Fig. Simulation output waveform for 1-bit ALU cell

Fig. 9 Schematic of proposed 1-bit ALU cell

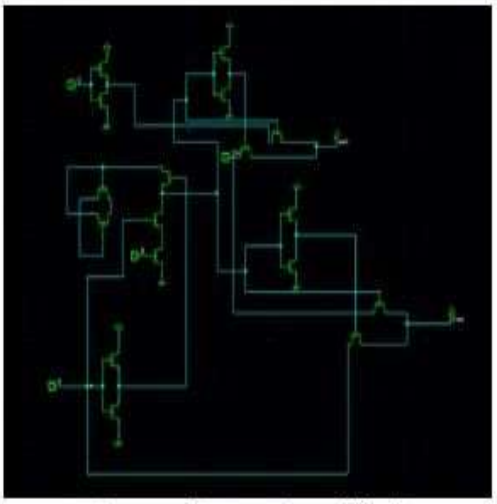

Fig. Schematic of proposed 17T full adder

andCompletesignforeachconceivablemixofsourcesof info.The recreation aftereffects of the proposed 1-digit ALU cell are shown in Fig. 10-11. The recommended ALU configuration beats the customary one since it utilizes lesspower andencountersless proliferationdelay. The qualities for every power utilization, delay, and relating power-postpone item for a few ideal plans are displayed in Table 2. North of a 100 ns run time, the poweraddressesthenormalofthewholetransientpower.

Along these lines, the postpone shows the typical spread deferralofthecontributiontoyieldsignalateachmoment duringatimeof100ns.Subsequently, it isobviousfrom thecomparisonof theresults that therecommended total snake

III. CONCLUSION

Wehaveanalyzedtheimplementationofafewfulladders and hybrid full adders that are currently in use in this discussion. In addition, all these snake networks require To disseminatethesignal, several interconnects or wires of different lengths are employed. This way, the proliferation times of theAggregate and Convey signals vary because of the varying RC delay along the channel. This will not be a problem when working with the slightestbitinputs,howeverwhenworkingwithmulti-bit inputs, these circuits will have critical detriments, for example, a higher convey proliferation delay, which influences the general speed of activity of the computerizedframeworkanyplaceitisbeingused.Also, there are two extra burdens to utilizing at least one rationale doors in the circuit to do the aggregate capability.

TABLE II. SIMULATION RESULTS (POWER IN e-6W, DELAY (units), AND PDP IN aJ) FOR DIFFERENT DESIGNS

Design	Power	Delay	PDP
FA-11T	16	64 ps	1024
HFA-22T	4.08	59.1 ps	241.1
*FA-17T	**1.16**	**9.52** ps	**11.04**
1-bit ALU [2]	4.47	20.33 ns	90.87
*1-bit ALU	**3.82**	**15.58** ns	**59.51**

Ourproposed17Tfullviper configurationtends toevery oneoftheseissues.Inaddition,wehavesurveyedvarious XOR doors and multiplexer plan to pick the best one. Finally, we havefostereda 1-digitALUcellutilizingthe proposed17Tfullviper,alowforeveryXORdoor,anda multiplexer in light of NMOS pass semiconductor rationale. This is then extended to an 8-bit ALU determined to boost a computerized processor's exhibition.Accordingtothereenactment discoveries,the recommended 8-digitALU diminishes the PDPby more than 52%, whiletheproposed 17T complete snakesaves 95.4% to 98%.

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