DESIGN OF 32-BIT VEDIC MULTIPLIER

[1]**K. Sai Sudheer,** Assistant Professor, Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P, India, Email id: saisudheer1978@gmail.com
[2]**G. N.V. Sushma,** Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P, India, Email id: sushmagelli2002@gmail.com
[3]**A. Sai Sowmya,** Department of ECE, Sri Vasavi Institute of engineering & Technology, Nandamuru, A.P, India, Email id: alapati134@gmail.com
[4]**P Naga Sailaja,** Department of ECE, Sri Vasavi Institute of engineering & Technology, Nandamuru, A.P, India, Email id: pnsailaja2002@gmail.com
[5]**P. Mani Babu,** Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P, India, Email id: manibabupuppala@gmail.com

Abstract
Multiply and Accumulate (MAC) is one of the primary operations used widely in signal-processing and other applications. Multiplier is the fundamental component of Digital Signal Processors (DSP's). Its parameters such as power, LUT utilization and delay decides the performance of a DSP. So, there is a need to design a power and delay efficient multiplier. In This paper, a 16-bit MAC unit is designed using an 8-bit Vedic multiplier and carry-save adder. It is compared with a conventional Booth multiplier. The entire design is implemented in Verilog HDL. Synthesis and simulations were done using Xilinx ISE Design Suite 14.5 and Vivado 2018.2.

1. Introduction

Multiplication Accumulation Unit (MAC) performs a vital position in Digital Signal Processing applications, microprocessor, multimedia etc. The main process of the Multiplication Accumulation Unit (MAC) is to multiply two numbers and add the obtained product in the accumulator. So, in VLSI circuits computation plays a crucial role as it decides the power consumption of the design. Power, area and time decides the efficiency of a Multiplication Accumulation Unit (MAC). The processes involved in the Multiplication Accumulation Unit (MAC) are multiplication and accumulation. Using Vedic's technique (Urdhva Tiryakbhyam sutra) the computation speed of multiplication is reduced far more than Wallace Tree multiplier and Booth's multiplier. Moreover, they consume more power and area compared to Vedic multiplier when implemented inside a Multiplication Accumulation Unit (MAC). So, the use of Vedic multiplier gives an added advantage for reduction of area and power in a MAC. This work demonstrates a 32 X 32 Vedic multiplier designed from the initial 2 X 2 Vedic multiplier which is developed using Vedic technique and then this Vedic multiplier is modified to develop a 4 X 4 module. It is then modified to develop an 8 X 8 Vedic multiplier. Later the designed unit is modified to develop a 16 X 16 Vedic multiplier and finally modifying it to a 32 X 32 block (all using Vedic techniques). The adder that is used in the addition process is Ripple Carry Adder (RCA). The designed MAC is implemented in a 4 tap FIR filter. The authors in [2] have designed a low power multiplier. It also reports good improvement in speed. The concept of parallel multiplication is used to attain speed. Significant improvements in power are obtained by performing some architectural modifications. High speed arithmetic operations are very important in many signal processing applications. Speed of the digital signal processor (DSP) is largely determined by the speed of its multipliers. In fact the multipliers are the most important part of all digital signal processors; they are very important in realizing many important functions such as fast Fourier transforms and convolutions. Since a processor spends considerable amount of time in performing multiplication, an improvement in multiplication speed can greatly improve system performance. Multiplication can be implemented using many algorithms such as array, booth, carry save, and Wallace tree algorithms. Booth algorithm reduces the number of partial products. However, large booth arrays are required for high-speed multiplication and exponential operations which in turn require large partial sum and partial carry registers. To improve the multiplication technique in processors like DSP or any other processors there is another technique taken from the ancient mathematics which is also called as Vedic mathematics.

Vedic Mathematics hails from the ancient Indian scriptures called "Vedas" or the source of knowledge. This system of computation covers all forms of mathematics, be it geometry, trigonometry or algebra. The striking feature of Vedic Mathematics is the coherence in its algorithms which are designed the way our mind naturally works. This makes it the easiest and fastest way to perform any mathematical calculation mentally. Vedic Mathematics is believed to be created around 1500 BC and was rediscovered between 1911 to 1918 by Sri Bharti Krishna who was a Sanskrit scholar, mathematician and a philosopher. He organized and classified the whole of Vedic Mathematics into 16 formulae or also called as sutras. These formulae form the backbone of Vedic mathematics. Great amount of research has been done all these years to implement algorithms of Vedic mathematics on digital processors. It has been observed that due to coherence and symmetry in these algorithms it can have a regular silicon layout and consume less area along with lower power consumption. The computational time required by the Vedic multiplier is less because the partial products are computed independently in parallel.

Arrangement of adders is another way of improving multiplication speed. Normally signal processing algorithms are developed using high level languages like C or Mat lab using floating point number representations. The algorithm to architecture mapping using floating point number representation consumes more hardware which tends to be expensive. Fixed point number representation is a good option to implement at silicon level. Hence our focus in this work is to develop optimized hardware modules for multiplication operation which is one of the most frequently used operation in signal processing applications like Fourier transforms, FIR and IIR filters, image processing systems, seismic signal processing, optical signal processing etc. Any attempt to come out with an optimized architecture for this basic block is advantageous during the product development stages. The advantage it provides over floating point multipliers is in the fact that Q format fraction multiplications can be carried out using integer multipliers which are faster and consume less die area.

2 Literature Survey

Design & implementation of area efficient low power high speed MAC unit using FPGA by [1] This paper illustrates the implementation of Multiply-Accumulate unit (MAC) to improve performance using the Ancient Indian Vedic Mathematics. Real-time signal processing needs high speed and high yield Multiplier-Accumulator (MAC) unit that consumes less power, which is always a key to achieve a high-performance digital signal processing system. Speed of the multiplier is essential to MAC unit. Vedic Mathematics is the ancient mathematics. There are sixteenth unique sutras in the Vedic mathematics. The Sutras saves effort and time required in solving the problems as compared to the formal methods. The Sutra [3] (Vertical and Crosswise) is used inside the MAC unit as a multiplier. The coding is done in VHDL, synthesis is done in Xilinx ISE series and the FPGA synthesis is done using Xilinx Spartan library. The results show that design of MAC unit using Vedic multiplication is much more efficient in terms of delay and speed compared to conventional multiplication.

Low power high speed multiplier using parallel multiplication by [6] This paper presents a low power and high-speed row bypassing multiplier. The primary power reductions are obtained by tuning off MOS components through multiplexers when the operands of multiplier are zero. Analysis of the conventional DSP applications shows that the average of zero input of operand in multiplier is 73.8 percent. Therefore, significant power consumption can be reduced by the proposed bypassing multiplier. The proposed multiplier adopts ripple-carry adder with fewer additional hardware components. In addition, the proposed bypassing architecture can enhance operating speed by the additional parallel architecture to shorten the delay time of the proposed multiplier. Both unsigned and signed operands of multiplier are developed. Post-layout simulations are performed with standard TSMC 0.18 μm CMOS technology and 1.8 V supply voltage by Cadence Spectre simulation tools. Simulation results show that the proposed design can reduce power consumption and operating speed compared to those of counterparts. For a 16×16 multiplier, the proposed design achieves 17 and 36 percent reduction in power consumption and delay, respectively, at the cost of 20 percent increase of chip area in comparison with those of conventional array multipliers. In addition, the proposed design achieves averages of 11 and 38 percent reduction in power consumption and delay with 46 percent

less chip area in comparison with those counterparts for both unsigned and signed multipliers. The proposed design is suitable for low power and high-speed arithmetic applications.

FPGA Implementation of Multiply Accumulate (MAC) Unit based on Block Enable Technique by [9] Power dissipation is one of the most important design objectives in integrated circuit, after speed. Digital signal processing (DSP) circuits whose main building block is a Multiply Accumulate (MAC) unit. High speed and low power MAC unit is desirable for any DSP processor. This is because speed and throughput rate are always the concerns of DSP system. This paper explores the design of low power MAC unit with block enable technique to reduce power dissipation. The whole MAC unit is implemented using 90-nm CMOS process technology. The whole MAC unit is operated at 314.268MHz with 1.5V supply voltage. The result analysis shows that the power consumption is reduced by using block enable technique.

A Reduce Bit Multiplication. [11] A reduced-bit multiplication algorithm based on the ancient Vedic multiplication formulae is proposed in this paper. Both the Vedic multiplication formulae, [12] are first discussed in detail. being a general multiplication formula, is equally applicable to all cases of multiplication. It is applied to the digital arithmetic and is shown to yield a multiplier architecture which is very similar to the popular array multiplier. Due to its structure, it leads to a high carry propagation delay in case of multiplication of large numbers. Nikhilam Sutra, on the other hand, is more efficient in the multiplication of large numbers as it reduces the multiplication of two large numbers to that of two smaller numbers. The framework of the proposed algorithm is taken from this Sutra and is further optimized by use of some general arithmetic operations such as expansion and bit-shifting to take advantage of bit-reduction in multiplication. We illustrate the proposed algorithm by reducing a general 4£4-bit multiplication to a single 2 £ 2-bit multiplication operation.

Power and Delay Efficient ALU Using Vedic Multiplier by [14] The power consumption and speed of a device is a crucial factor as most of the designs move towards the system-in-package and system-on-chip products. As the size of the device scale down, speed and power consumption doesn't go hand in hand. Switching power in a CMOS circuit is a prime component of the total power consumption. This switching power is caused by simultaneous charging and discharging of the load capacitances when the signal undergoes transition. The speed of a digital circuit is determined by how fast the circuit can generate outputs from the given inputs. There are various ways to reduce power consumption such as voltage scaling, clock gating, reversible logic, and so on. For increasing the speed of a circuit, delay inside the logic should be reduced. The choice of a smarter design architecture helps in improving the circuit speed. This work focuses on an ALU design using Vedic algorithm and reversible logic. It aims for better speed and power. The proposed Vedic algorithm based ALU design yields 6.7% decrease in dynamic power and 2.2% decrease in a number of cells used.

3 Proposed System

The concept of the carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result with single or multiple stages. In carry-select adders both sum and carry bits are calculated for the two alternatives: carry "0" and "1". Once the carry-in is fired, the correct computation is chosen using multiplexers to produce the desired output. Therefore, instead of waiting for the carry-in to calculate the sum, the sum is correctly output as soon as the carry-in gets there. The time taken to compute the sum is then avoided which results in a good improvement in speed.

Here, four 4X4 Vedic multiplier blocks and three carry select adders of 8 bits each are used. The arrangement of the carry select adders is made in a different way such that it requires less computation time. Some of the carry select adders are given with zero inputs, wherever required. The output of middle multipliers is added using first CSLA. The Output of first CSLA and first Vedic multiplier are added using second CSLA. Carry outputs from first two CSLAs are performed by OR operation and it is given as an input to the third CSLA to generate the final result

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The design of 16×16 block is a similar arrangement of 8×8 blocks in an optimized manner which is shown in Figure 5.The first step in the design of 16×16 block will be grouping the 8 bit (byte) of each 16-bit input.The LSB of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 8×8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are added in a 16-bit carry select adder optimally to generate final product bits. The schematic of a 16×16 block is designed by using the 8X8 Vedic multiplier. The partial products represent the Urdhva vertical and cross product terms. Then by using or gate, the final product is obtained

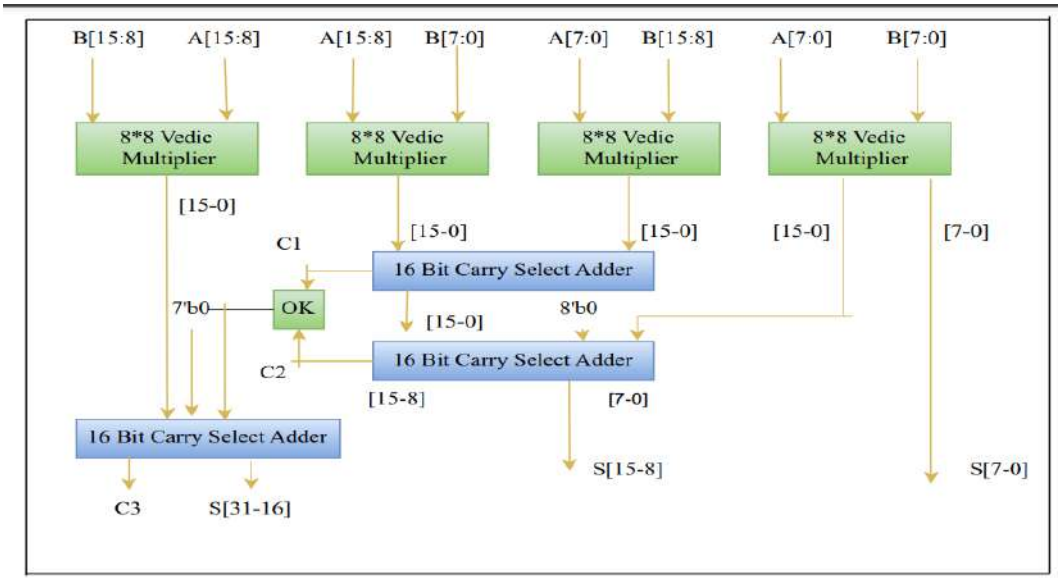

Figure 1. Block Diagram of 16X16 bit Vedic Multiplier

The use of carry select adder increases the hardware thereby more power consumtion which is twice that of ripple carry adder. The use of multiplexer increases the chip area. But considerable increase in the speed is achieved. So, optimization of the carry select adder can be useful in increasing the speed of the multiplier speed.

Results

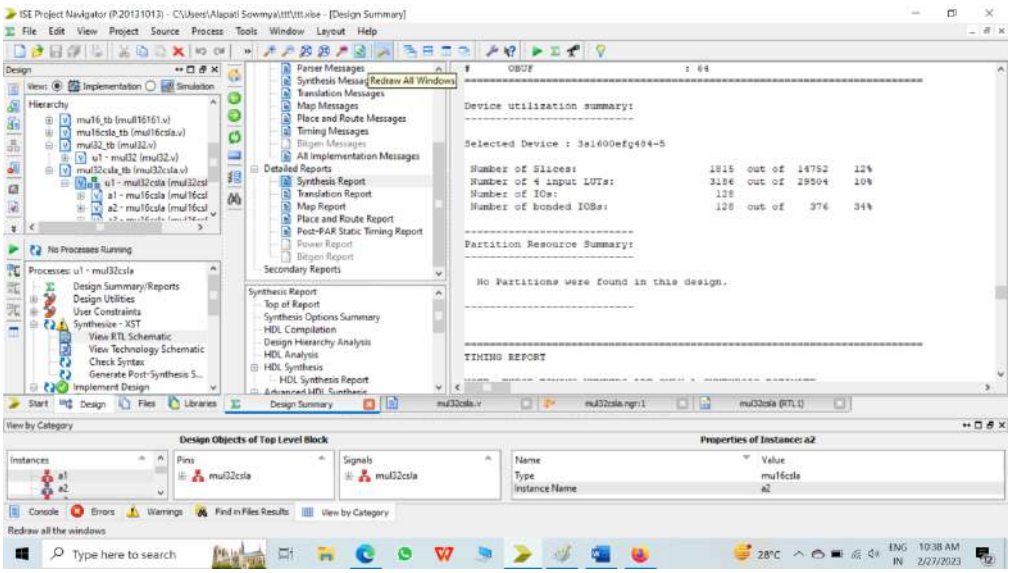

Fig2 Utilization of 32 bit MAC multiplier

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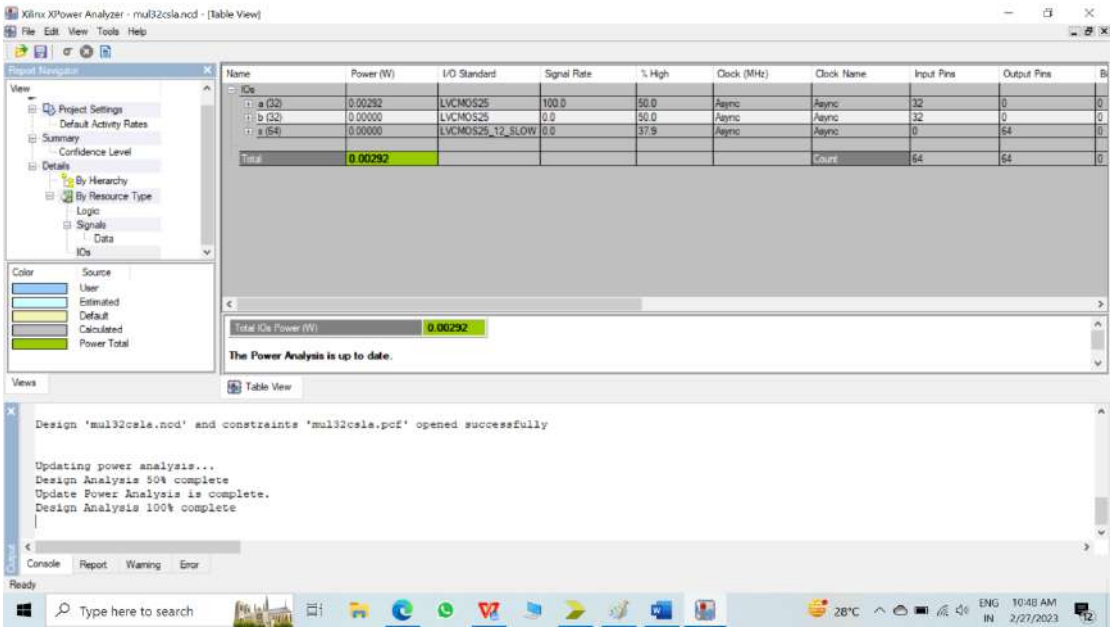

Fig 3 Power delay of 32 bit MAC Multiplier

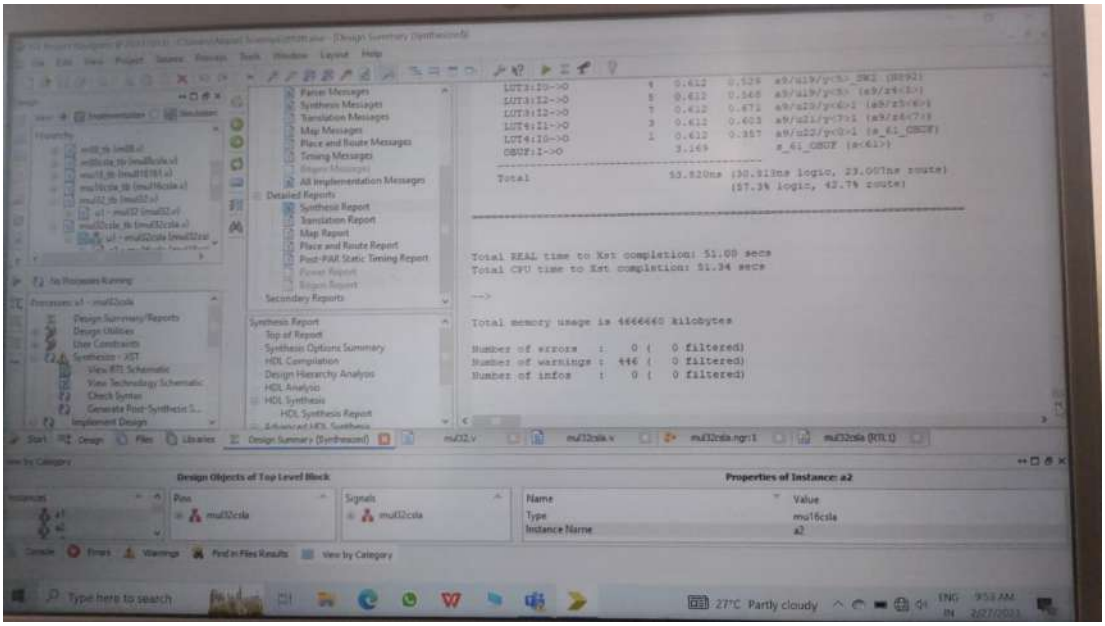

Fig 4 Time delay of 32 bit MAC Multiplier

Conclusion

A MAC unit is realized using Verilog and the synthesis is done in xilinx. A comparison is carried out with the MAC used in [1]. Power and area reductions have been reported. The power has been reduced by 9% and area by 5%. Also, the proposed MAC is utilized in 4 tap FIR filter. It highlights significant improvements in power and area. As a future scope the designed MAC can be implemented in an IIR filter. Also, implementation of MAC using other Vedic techniques is asuitable choice. This project presents a highly efficient method of multiplication – "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It gives us method for hierarchical multiplier design and clearly indicates the computational advantages offered by Vedic methods. Hence our motivation to reduce delay is finely fulfilled. Future work lies in the direction of introducing pipeline stages in the multiplier architecture for maximizing throughput and also, we can implement for 64 – bit also.

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