

## QCA BASED COST-EFFICIENT CODE CONVERTERS WITH TEMPERATURE STABILITY

**Mr.N.Nagaraju**, Assistant Professor, Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P, India,, Email id: dsp.nagarajunalluri@gmail.com  
**A. Rani**, Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P, India, Email id: raniakuri783@gmail.com  
**S.Teenasri**, Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P,India, Email id: sontiteenasri@gmail.com  
**B.B.subrahmanyam**, Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P, India, Email id: bogireddysubrahmanyam@gmail.com  
**P.S.V.V.Srisha**, Department of ECE, Sri Vasavi Institute of engineering &Technology, Nandamuru, A.P, India, Email id: satyapeddireddy2002@gmail.com

### ABSTRACT

Quantum dot Cellular Automata(QCA) area prominent nano technology that is widely employed in digital circuits and systems. In comparison to complementary metal–oxide semi conductor(CMOS) technology, QCA is a remarkable and challenging alternative with many attractive aspects such as fast execution and low power use. To accomplish all arithmetic processes, code converters are the fundamental unit of information change. Most of the converters, out of many designed for far in QCA, did not considered temperature stability, energy dissipation which may contribute to propagate as a non-operational circuit in various temperatures. This paper proposes a novel concept for a binary-to-gray code and a BCD-to-Excess 3 code converter based on QCA. The promised structure diminishes the number of cells, area utilized to make the design cost effective. The fundamental purpose of this research is to give a temperature stability. The operability of the introduced designs and temperature stabilities are verified with the QCADesigner2.0.3 tool.

**Keywords:** Quantum Cellular Dot Automata, Gray code, Binary code BCD Excess3 code, Temperature Stability.

### 1. Introduction

Quantum-dot cells are key components of QCA technologies to implement as Logic Gates, Wires, and Memories. The basic logic elements in QCA technology are the Majority gate and Inverter. Wires can be used for signal propagation in QCA circuits. Logic elements viz; AND gate & OR gate can be obtained by manipulating the Majority gate. Though the technology is different from convention CMOS designs, it is effective and realistic to implement the low power logic circuits. Thus, QCA is a new innovation at Nano-scale and an appealing substitute to ordinary CMOS. It is a possible technology for the next generation of digital circuits and systems and widely utilized as a part of advanced frame works. Quantum-speck cell automata is a processing world view utilizing varieties of nano structures called quantum spots Quantum dots are nano structures made from standard semi conductive materials, for example, Si/SiO<sub>2</sub>. These structures can be displayed as 3-dimensional quantum wells. Accordingly, they show novality quantization impacts even at separation safe hundred times bigger than a material's grid steady.

A quantum speck can in reality be pictured as a well. Electrons, once caught inside the speck, don't the only one have the vitality required to get away. We can utilize quantum material science further bolstering our good fortune in light of the fact that the littler a quantum speck is physically, the higher the potential vitality important for an electron to get away.

The technology, CMOS is arriving at the physical pick margin after which any additional downscaling in dimension is a concern of possibility. High power consumption, high leakage current, and high-

density design scale the performance of CMOS. A promising and acceptable technology with the capability to outperform these loopholes is highly demanded. One such nanotechnology, the QCA, is found suitable for designing the structure to reduce cost and enhance energy-efficiency [1,2]. The striking features like low power consumption in signal propagation, fast and high density design have attracted researchers to look into the requirements of its visibility and implementation [3]. A QCA cell is accounted of a couple of free electrons, confined inside the well potential. Not likely the conventional CMOS technology, instead of any current flow, signal transfer and propagation occurs under external clock signal operation in QCA. A polarized cell state is passed on via QCA wire to transfer the data with assist of the four-phase clocking system [4]. There exists enormous QCA based research work in every section of digital logic. It does not exclude one of the essential sections, a code converter [5]. Code converters are useful circuit that converts from one code to another which is programmed in the logic array and utilized in many areas, like data protection and increment data adaptability [5]. Excess-3 code and Gray code are non-weighted code with self complementary and cyclic code in nature respectively. The earlier proposals have focused on designing converter in QCA with a reduction in cell number or area. Most of the work does not propose any design for gray to binary converter. In no design in the literature have important features like the feasibility of working under various temperatures and the amount of energy dissipated from the circuit. This somehow strikes the momentum of the work in this paper

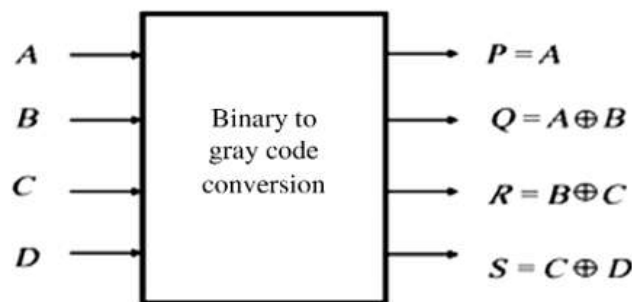
## 2. LITERATURE SURVEY

Quantum dot cellular automata (QCA), is known as high speed low area/power nano scale technology .Simple QCA circuits (e.g., a full adder) have already been fabricated and more complex designs have been simulated via QCA design tools(e.g., QCA Designer ). A primitive QCA cell contains four electron place holders (aka dots) that can accommodate two repulsive electrons on one of the dot pairs on the same diameter. depicts an empty QCA cell (a), a one with two electrons on slash-oriented diameter that represents the low logical state 0 (b), and a backslash one that represents the logical state 1(c). Also, the functions of a majority gate and a robust inverter are illustrated in d, and e, where sample input values and the corresponding output values are indicted. Majority gate is the basic QCA component that together with inverter gate constitute a complete logic set, since AND and OR gates can be defined in terms of partially utilized majority gate, where one input is 0 and 1, respectively. Many logical circuits that have been realized in CMOS, including those of computer arithmetic circuits are also realized in QCA platform. Instead of trivial mapping of AND/OR gates to partially utilized majority gates, one can reformulate the logical expressions of the corresponding CMOS designs in terms of maximizing the use of fully utilized majority gates. This is generally expected to lead to less number of total majority gates. The previous designs in the context of code converters. It includes Binary to Gray converter as well as BCD to Excess3 converters. A conversion circuit should be planted connecting the pair of systems when they use various codes for standardized information. In this way, a code converter circuit forms the pair of systems perfect even though each one an alternate binary code. In this regard, numerous research has taken place for the implementation of the convertors as discussed below. Several research articles have been reported for the method of designing binary to gray code converter. In this design reported that, the circuit is nor expandable or scalable. An xor based design of converter has been reported. The use of a signal distribution network for the design was proposed however, it was not properly used in the QCA implementation. A similar design can be reported in with low energy consumption analysis. A new XOR gate is presented in QCA and a different layout for binary to gray code is also presented using multi-layer cross over technique. However, no design was found in the literature to propose the design to get back the binary value in return, i.e. gray to binary converter. The concept of energy dissipation was introduced but without any proper illustration. The temperature stability factor still remains an issue to be addressed. Along with the converter for the conversion of binary to gray code, a similar type of purpose i.e. binary to excess-3 code conversion is also practiced in QCA, popularly known as BCD to Excess-3 code converter. A design for BCD to Excess-3 code converter in QCA is proposed in using multi-layer approach. It is not considered to be a suitable candidate for the fabrication. A coplanar approach for the BCD to excess-3 code converter circuit can be found, which used the simple QCA logic circuit using NAND and NOR. Whereas, another coplanar design with a modified logic in the circuit, but suffered with issues like cell count,

area and scalability. At the same, no design in the literature have concentrated on temperature variable applicability and energy dissipation. Moreover, the mentioned works have concentrated in the concise design, restricted to cell count only. No such design has been reported to describe the feasibility of working on the design in various temperature. Additionally, the energy dissipation for the converter design was ignored in most of the previous cases. As each and every code use two couple of bits for representing a decimal digit, 4(four) input and 4(four) output variables must be there is reported. These lead us to design a cost-effective converter and analysis of temperature stability.

### 3. Methodology

In this section, the design principle and the QCA layout for the converters are discussed. The simulated results are also illustrated to establish the functionality of the proposed design. The QCA computation proceeds by cell direction dependent on neighboring cell polarization. Estimates are designed for understanding the appropriate techniques and promoting the strategy proposed QCA Designer 2.0.3 is chosen at that level & that simulation method is described in QCA Designer 2.0.3 reinforces the usefulness of the aim, which contains default values such as cell size, reduces impact, total relaxation time, relative primitively, etc. Code converters are Circuits for interpreting a provided code into another, which is concealed in the logical array & run in a few regions to enhance the adaptability for information and hold outsiders informed. Binary code is how communication takes place and obtains user data using the number system. For example, the seven-bit binary sequence 1,100,100 is identical to the decimal number 100. Gray code, being a numeral scheme, is defined by differing each value only by a single number from the previous number. Gray code is a numeral structure program where each value differs from the previous number. The gray code, which functions as an analog-to- digital converter has various useful uses; simplifies fault detection and peripheral tools.



**Fig1:** Block Diagram of 4-bit Binary to Gray Code Converter

#### Truth Table of Binary to Gray Code Converter:

The below table shows the truth table of binary to gray code converter

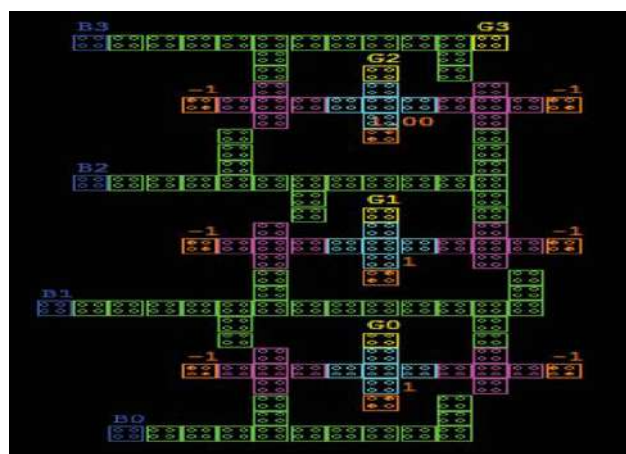
**Table1:** Truth Table of 4-bit Binary to Gray Code Converter

| Binary Inputs |    |    |    | Gray Outputs |    |    |    |
|---------------|----|----|----|--------------|----|----|----|
| B3            | B2 | B1 | B0 | G3           | G2 | G1 | G0 |
| 0             | 0  | 0  | 0  | 0            | 0  | 0  | 0  |
| 0             | 0  | 0  | 1  | 0            | 0  | 0  | 1  |
| 0             | 0  | 1  | 0  | 0            | 0  | 1  | 1  |
| 0             | 0  | 1  | 1  | 0            | 0  | 1  | 0  |
| 0             | 1  | 0  | 0  | 0            | 1  | 1  | 0  |
| 0             | 1  | 0  | 1  | 0            | 1  | 1  | 1  |

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

**QCA Implementation of Binary to Gray Code Converter:**

The below figure shows the QCA implementation of Binary to gray code converter

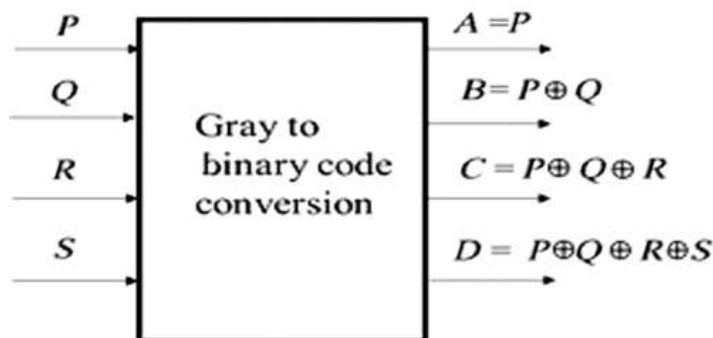


**Fig2:** QCA Implementation of Binary to Gray Code Converter

In this we are going to discuss about how QCA implemented and with simulation results

**Block diagram of Gray to Binary Code Converter:**

The below diagram shows the block diagram of gray to binary code converter



**Fig3:** Block Diagram of Gray to Binary Code Converter

**Truth Table of Gray to Binary Code Converter:**

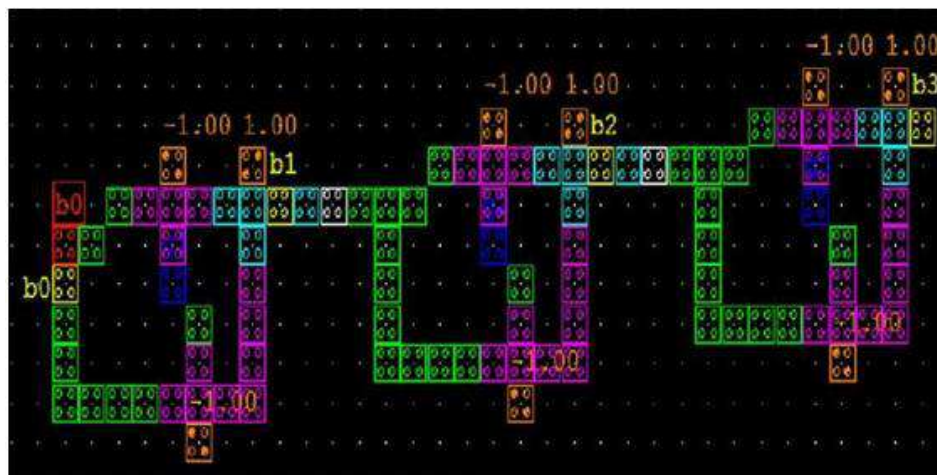
**Table2:** Truth table of gray to Binary code converter

| Gray Inputs |    |    |    | Binary Outputs |    |    |    |
|-------------|----|----|----|----------------|----|----|----|
| G3          | G2 | G1 | G0 | B3             | B2 | B1 | B0 |
| 0           | 0  | 0  | 0  | 0              | 0  | 0  | 0  |

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

**QCA Implementation of Gray to Binary Code Converter:**

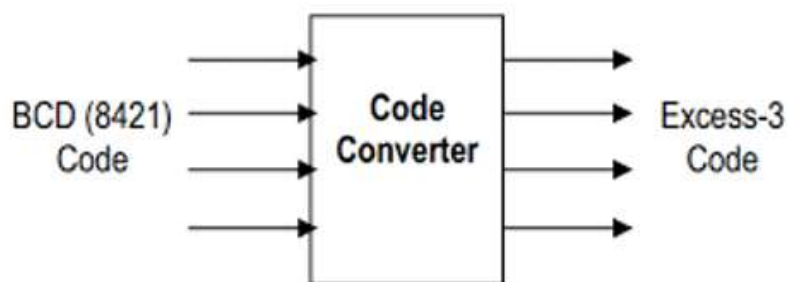
The below figure shows the QCA implementation of gray to binary code converter



**Fig4:** QCA Implementation of Gray to Binary Code Converter

**Block diagram of BCD to Excess-3 Code Converter:**

The below diagram shows the block diagram of BCD to Excess-3 code converter



**Fig5:** Block diagram of BCD to Excess-3 code converter



**Truth table of BCD to Excess-3 Code Converter:**

**Table3:** Truth table of BCD to Excess-3 Code Converter

| BCD Inputs |    |    |    | Excess-3 Outputs |    |    |    |
|------------|----|----|----|------------------|----|----|----|
| B3         | B2 | B1 | B0 | E3               | E2 | E1 | E0 |
| 0          | 0  | 0  | 0  | 0                | 0  | 1  | 1  |
| 0          | 0  | 0  | 1  | 0                | 1  | 0  | 0  |
| 0          | 0  | 1  | 0  | 0                | 1  | 0  | 1  |
| 0          | 0  | 1  | 1  | 0                | 1  | 1  | 0  |
| 0          | 1  | 0  | 0  | 0                | 1  | 1  | 1  |
| 0          | 1  | 0  | 1  | 1                | 0  | 0  | 0  |
| 0          | 1  | 1  | 0  | 1                | 0  | 0  | 1  |
| 0          | 1  | 1  | 1  | 1                | 0  | 1  | 0  |
| 1          | 0  | 0  | 0  | 1                | 0  | 1  | 1  |
| 1          | 0  | 0  | 1  | 1                | 1  | 0  | 0  |

**QCA Implementation of BCD to Excess-3 Code Converter:**

The below figure shows the QCA implementation of BCD to Excess-3 code converter



**Fig6:** QCA implementation of BCD to Excess-3 code converter

**Temperature stability for Code Converters:**

The pattern was tested for operation by implementing the Simulation Engine setup as “Coherence Vector” in the QCA Designer tool instrument under a temperature range starting from 1 K to 16 K.

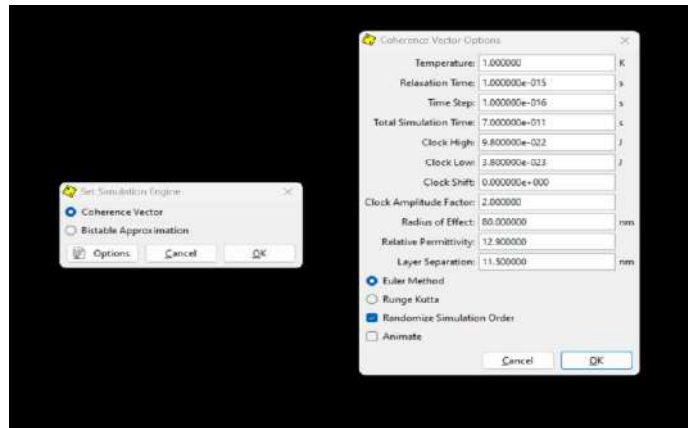


Fig7: Temperature stability for all code converters

**Results:**

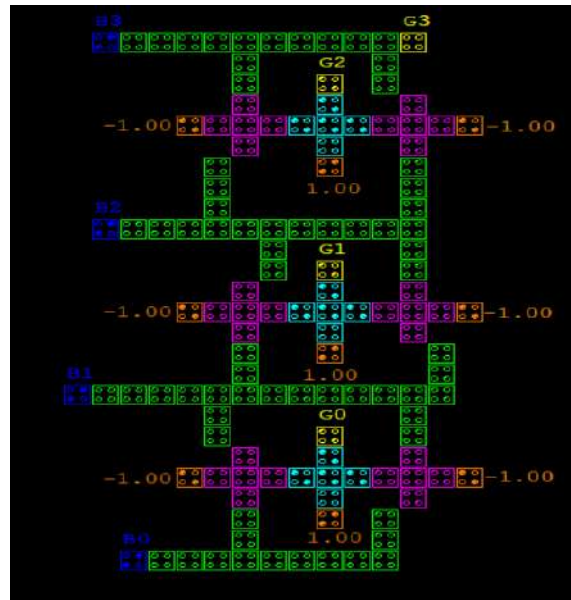


Fig8: QCA Design for binary to gray code converter

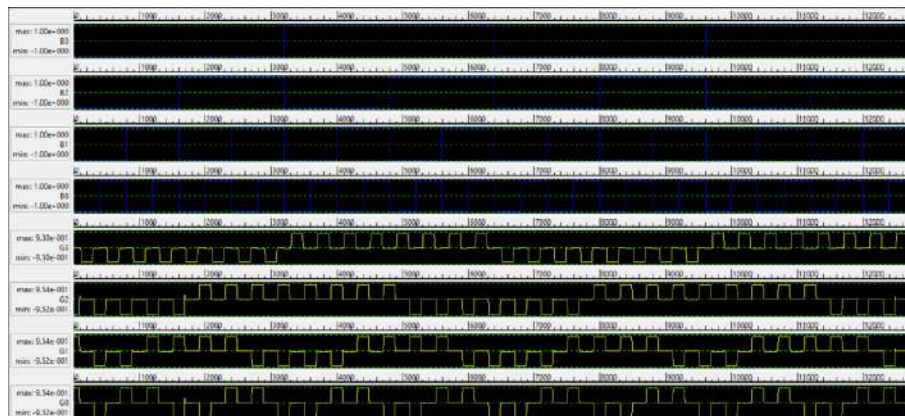


Fig9: QCA simulation for binary to gray code converter



Fig10: QCA design of gray to binary code converter



Fig11: QCA simulation of gray to binary code converter

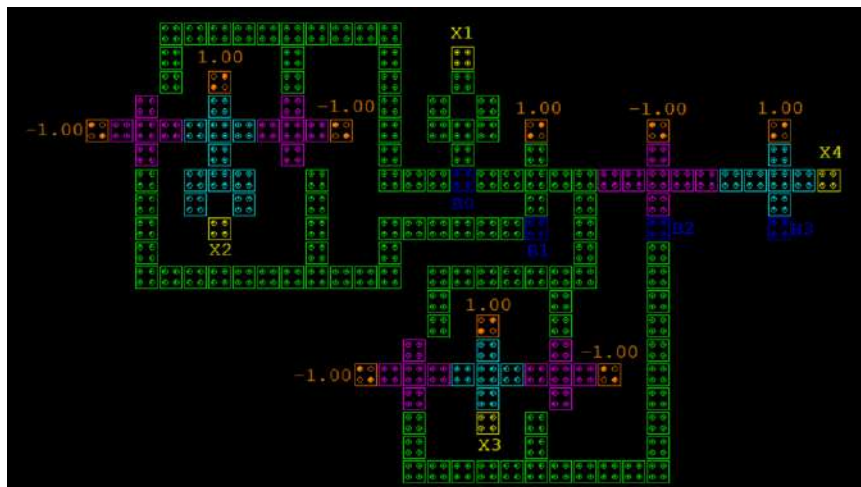


Fig12: QCA Design for BCD to Excess-3 code converter

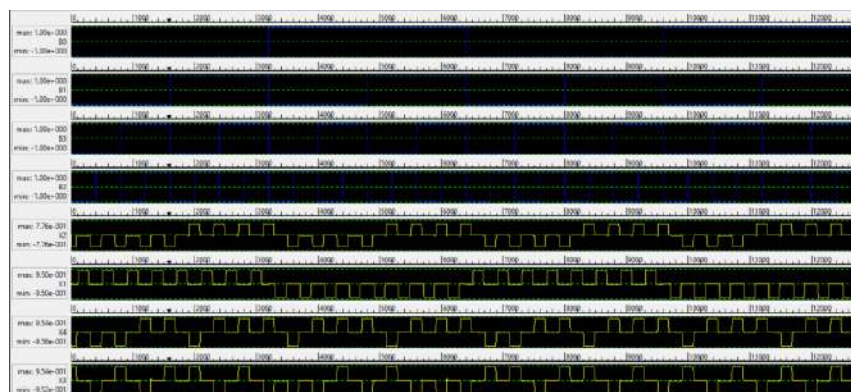


Fig13: QCA simulation for BCD to Excess-3 code converter



**Temperature stability for Code Converters:**

| Temperature(k) | Operation status |
|----------------|------------------|
| 1              | Functional       |
| 2              | Functional       |
| 3s             | Functional       |
| 4              | Functional       |
| 5              | Functional       |
| 6              | Functional       |
| 7              | Functional       |
| 8              | Functional       |
| 9              | Functional       |
| 10             | Functional       |
| 11             | Functional       |
| 12             | Functional       |
| 13             | Functional       |
| 14             | Functional       |
| 15             | Functional       |
| 16             | Functional       |
| 17             | Not Functional   |
| 18             | Not Functional   |
| 19             | Not Functional   |
| 20             | Not Functional   |

**Table4: Results for Temperature stability of code converters**

**Conclusion**

Cost effective design of Binary to Gray code design is proposed. It also proposed a Gray to Binary code converter which confirms the acceptability of the code converted in its counter design (Binary to Gray). An extensive comparison has been carried out for all the proposed designs with the previous designs. It can be noticed that, the designs outperformed the previous design in metrics like majority gate, latency, area as well as cross over. Apart from that, the study also includes different operational parameters such as Energy dissipation, Temperature Stability. There analysis complies that, the stable temperature regions for in which the respective proposed circuits for the Binary to Gray code circuit the TSF-MAX polarizations range is 1k to 16k and TSF-MIN polarization range is 1–16k, in case of Gray Code to Binary converter the measure for the same is recorded as 1–16 k. The result for Binary to Excess-3code converter shows both TFS–MAX & TFS–MIN polarization is 1–16k. The proposed designs were simulated using QCA-Designer 2.0.3 The circuits will hold

their operational stability on exceeding their respective stable ranges during sole implementations, but operating in the stable range will enable best output polarizations with the least amount of dissipation when they are integrated with other circuits.

## References

- [1] D.Abedi and G.Jaberipur, "Decimal Full Adders Specially Designed for Quantum-Dot Cellular Automata," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. PP, no. 99, pp. 1–5, 2019.
- [2] V. Pudi and K. Sridharan, "New Decomposition Theorems on Majority Logic for Low-Delay Adder Designs in Quantum Dot Cellular Automata," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 59, no. 10, pp. 678–682, Oct. 2019.
- [3] Y. Zhang, G. Xie, M. Sun, and H. Lv, "Design of normalised and simplified FAs in quantum-dot cellular automata," *J. Eng.*, vol. 1, no. 1, pp. 1–9, 2020.
- [4] M. Balali, A. Rezai, H. Balali, F. Rabiei, and S. Emadi, "Towards coplanar quantum-dot cellular automata adders based on efficient three-input XOR gate," *Results Phys.*, vol. 7, pp. 1–9, 2020.
- [5] H. Rashidi and A. Rezai, "High-performance full adder architecture in quantum-dot cellular automata," *J. Eng.*, vol. 1, no. 1, pp. 1–9, Jun. 2021.
- [6] R. Jaiswal and T. N. Sasamal, "Efficient design of full adder and subtractor using 5-input majority gate in QCA," in *10th International Conference on Contemporary Computing (IC3)*, 2021, pp. 1–6.
- [7] S. R. Heikalabad, M. N. Asfestani, and M. Hosseinzadeh, "A full adder structure without cross-wiring in quantum-dot cellular automata with energy dissipation analysis," *J. Supercomputers*, vol. 74, no. 5, pp. 1994–2005, 2021.
- [8] D. Mokhtari, A. Rezai, H. Rashidi, F. Rabiei, S. Emadi, and A. Karimi, "Design of Novel Efficient Full Adder Circuit for Quantum dot cellular technology".
- [9] M. Naji Asfestani and S. Rasouli Heikalabad, "A unique structure for the multiplexer in quantum-dot cellular automata to create a revolution in design of nano structures," *Phys. B Condens. Matter*, vol. 512, no. January, pp. 91–99, 2021.
- [10] H. Rashidi, A. Rezai, and S. Soltany, "High-performance multiplexer architecture for quantum-dot cellular automata," *J. Comput. Electron*, vol. 15, no. 3, pp. 968–981, 2021.
- [11] S. Singh, S. Pandey, and S. Wairya, "Modular Design of 2 n: 1 Quantum Dot Cellular Automata Multiplexers and its Application, via Clock Zone based Crossover," *Int. J. Mod. Educ. Comput. Sci.*, vol. 8, no. 7, pp. 41–52, 2021.
- [12] H. Rashidi and A. Rezai, "Design of Novel Efficient Multiplexer Architecture for Quantum-dot Cellular Automata," *J. Nano- Electron. Phys.*, vol. 9, no. 1, pp. 1012–1–1012–7, 2022.
- [13] A. Kamaraj and P. Marichamy, "Design and implementation of arithmetic and logic unit (ALU) using novel reversible gates in quantum cellular automata," in *4<sup>th</sup> International Conference on Advanced Computing and Communication Systems (ICACCS)*, 2022, pp. 1–8.
- [14] M. Rahimpour Gadim and N. Jafari Navimipour, "A new three-level fault tolerance arithmetic and logic unit based on quantum dot cellular automata," *Microsyst. Technol.*, pp. 1–11, Aug. 2022.
- [15] M. G. Waje and P. K. Dakhole, "Design and implementation of 4-bit arithmetic logic unit using Quantum Dot Cellular Automata," 2022, pp. 1022–1029.