"High-Performance 1-Bit Hybrid Full Adder with Optimized Power and Speed

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Abstract— CCMOS, transmission gates, and pass transistor reasoning are the bases of the hybrid new FA design. Existing CCMOS is compared with this hybrid FA. For this purpose, the circuit analysis is done using the Cadence toolkit. There are twenty different FA circuits that are used in different applications. The two designs' performances are compared. To demonstrate scalability, the designed FA has also been scaled up to a word length of 64 bits. With the word size increased to 64 bits, only five of the ten designs other than the designed FA are able to work without a buffer in the intermediate stages. Simulation results reveal that the proposed topology performs remarkably in terms of power consumption and delay, which essentially confirms the low power delay product.

Key Words— 1-bit full adder, CMOS technology, PDP, ALU, Scalable Architecture.

I. INTRODUCTION

Improvement in scaling has rapidly improved transistors that have led to greater interest in the design of microelectronic circuits using less power. The nature will enhance the need for circuit design with more performance microelectronic circuit. Large arithmetic scale in most applications such as DSP chips, image, video processing, and other computations can use a microprocessor. Of these, addition is among the simplest operations performed mostly. It is therefore critical to binary addition to use the 1-bit Full Adder (FA), which forms the fundamental building block for wide word-length adders. Hence, the need to raise microprocessors' ALU efficiency requires optimization of the FA's performance. The present paper suggests a novel hybrid FA based on PTs, TGs, and static CMOS logic. The designed FA is implemented using 45 nm technology based on Cadence tools. To check the validation of the designed design, the performance metrics have been compared against twenty existing FA designs providing supply voltages ranging between 0.4 V and 1.2 V. The architecture emphasizes scalability, low power consumption, and minimal propagation delay. It is thus ideal for high-frequency and power-sensitive applications. Simulation results indicate that the proposed hybrid full adder is superior to conventional designs in terms of PDP and computing speed, suggesting it could be used in modern digital systems.

II. RELATED WORK

One logic style used by 12- Transistor, Complementary Pass Transistor Logic, and traditional CMOS (CCMOS) logic based FA [7]. Therefore, buffers are necessary to achieve the supply voltage level of the signal when the degradation of voltage will occur in CPL logic style. Voltage issue does not affect the CCMOS FA. Nevertheless, the major weak point of the CCMOS FA is its high input impedance.

Recently, the best features of several logic models have been merged into one FA cell by a hybrid design approach combining several logic models. The Transmission Function Adder (TFA) of the study uses TGs [10]. The TG Adder (TGA) of [8], [9] uses TGs. Although TGA and TFA FA do not have this problem, these two adders are a serious problem when these have limited capacities.

Other methods that have been researched to address these limitations include pass-transistor logic (PTL) and transmission gate logic. Rather than connecting two independent two-input XOR gates in cascade, the 24-T FA directly computes sums by an XOR gate of three inputs. Before that, the input bits of a 14-T and 10-T FA are processed using an XOR gate. In contrast, transmission gate logic increases the area and complexity of the circuit but provides efficient signal transfer. The very low count of transistors makes up very little of the surface area. Still, their ability to drive remains a concern; their use is still quite restricted in crowds.

III. FULL ADDER DESIGN APPROACH

The design process used for the generated FA is shown in Fig. 1. The proposed FA consists of four major modules, two of which are for sum and the other two for carry generation. The designed schematic is displayed in Fig. 2.

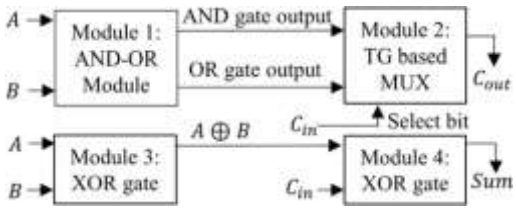

Fig. 1. Block diagram of designed full adder.

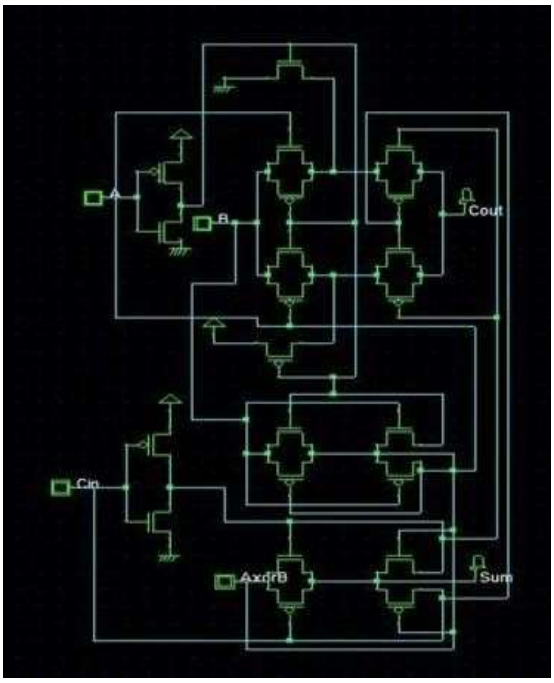

Fig. 2 Schematic of the designed FA.

The hybrid full adder with a single-bit implementation in the current architecture was due to the derivation. The hybrid design offers outstanding speed, power, and efficiency compared to any other conventional adders. The most of the techniques which have been used in the system are based on nm technology.

The following names are used to describe the carry and sum generating components, hybrid FA architecture. So far, two major achievements of VLSI design circuits are in increasing speed while reducing power consumptions and transistor size. In its small size, the designed solution made use of CMOS technology to be powered.

IV.

SIMULATION DISCUSSION AND RESULTS

The performance metrics have been analyzed using simulation on the GPDK 45 nm technology node. This was done using Cadence simulation tools. Buffers have been added to the input and output sides of the simulation test bench. On the output side, there was also a 6 fF load capacitance. This causes major signal distortion in the circuit compared to a realistic setting. Consequently, under this configuration signal distortion seen in the circuit would be pretty severe compared with the actual world. FAs have been applied for sizing transistor using particle swarm optimization method [23]–[24]. If we apply the swarm algorithm for sizing the transistors, then the problem statement will be represented by the vector $\bar{\bar{W}}_{\bar{m}\times\bar{n}}\rightarrow$, where n is the number of particles and m is the number of transistors. Each particle has three different inclinations in the search space: (a) the natural tendency toward inertia, (b) the highest value that any particle can have, and (c) the best value that a team has achieved. The transistor width is randomly changed from the smallest to the largest size that can be utilized in order to replicate that circuit. A low Power Delay Product, or PDP, is the aim here.

A. Performance of FA cells for various supply voltage

Table I reports the post-layout simulation results for the suggested full adder (FA) design. These are PDP, delay, and power consumption. As can be seen from the above results, the proposed FA has a higher latency and PDP value than the others. Though its power consumption is not the least in all of the designs under comparison, still, the power performance is reasonably low to be used practically in modern CPUs. The inability of these designs to work at low voltages highlights the robustness and efficiency of the proposed FA, which has achieved reliable operation at 0.4 V while maintaining competitive performance metrics. This makes the proposed FA suitable for low-power, high-performance applications in advanced digital systems.Another simulation has also been carried out with the applied voltage ranging from 0.45 V to 0.75 V to find out their minimum operating voltages of these FAs. Delay for FA cells also was found to increase sharply when they start operating at supply voltages less than 0.8 V. In order to obtain the desired performance for more aggressive technologies, the connection width should be an optimization target parameter.

B. Performance of FAs operating in cascade

To verify scalability, FAs are expanded to 4, 8, 16, 32, and 64 bits in the manner of the Ripple Carry Adder, as depicted in Fig. 4 [18]. FA cascades do not contain any buffer between them. The simulation results for the performance parameter are presented in Table II. It has been seen that only five of the twenty FAs in use at present will be available upon the 64-bit extension. GDI D1 [22], Hybrid 2 [18], and Hybrid 6 [21] all showed excellent FA performance at the single-cell level. They can only be expanded by eight bits, though. This occurs due to the degradation of the signal (voltage) over several stages of propagation.

Vdd and Gnd are used to create output signals for CCMOS FAs due to the logic structure at the output terminals, which is based on CCMOS. This prevents voltage degradation in long carry chains for 24-T [11] and CCMOS [7] FAs by rejuvenating the voltage at each stage.

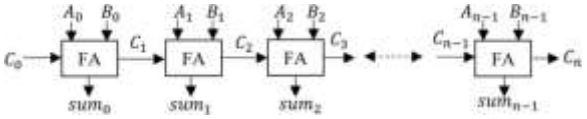

Fig. 3. Implementation of n-bit adder using 1-bit FA.

New-HPSC [16] and HPSC [14] Since the output terminals of the proposed design employ the CCMOS logic, FAs could not work in 64-bit. This is because they took a long time to reach the input frequency (100 MHz). The output terminals of Hybrid , GDI, and GDI D3 FAs are not using the CCMOS logic. However, in their inherent design characteristics, they allowed the 64-bit operation. The word level involves adding additional inputs with words An and Bn as shown in Fig. 3.

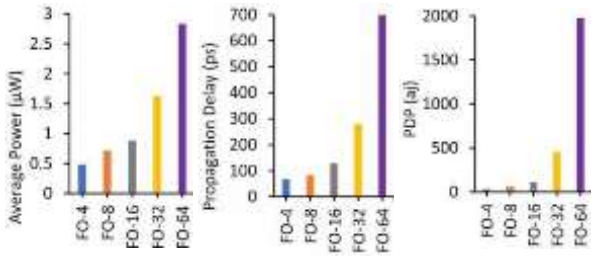

Fig. 4. Performance of FA under various loads with 0.8 V supply voltage.

TABLE I
PERFORMANCE OF FULL ADDER CELLS UNDER VARIOUS SUPPLY VOLTAGE

TC: Transistor Count, AP: Average Power, DP: Dynamic Power (Switching Power + Short-Circuit Power), PDP: Power Delay Product, SP: Static Power, F: Failed to Operate, PR: Performance Ratio (Proposed FA Value: Best Value Obtained by Other FAs)																	
Full Adder	**Ref. no**	**T C**	**Power (AP in µW, DP and SP in nW)**									**Delay (ps)**			**PDP (aJ)**		
			0.4 V			**0.8 V**			**1.2 V**			**0.4 V**	**0.8 V**	**1.2 V**	**0.4 V**	**0.8 V**	**1.2 V**
			AP	**DP**	**SP**	**AP**	**DP**	**SP**	**AP**	**DP**	**SP**						
CPL	[5]	32	0.488	458.2	29.8	1.72	1612.8	107.3	3.89	3634.1	255.9	612.1	84.8	37.3	298.7	145.9	145.1
12-T	[6]	12	F	F	F	1.2	1158.4	41.6	2.54	2423.4	116.6	F	447.4	67.6	F	536.9	171.7
CCMOS	[7]	28	0.159	149.1	9.9	0.68	660.3	19.7	1.91	1841.6	68.4	809.3	125.8	39.7	145.7	85.5	75.8
TGA	[8]	20	0.163	158.8	8.2	0.64	617.4	22.6	1.41	1365.8	44.2	893.4	139.7	58.3	151.9	89.4	82.2
TFA	[10]	16	0.155	150.9	8.1	0.61	586.5	23.5	1.33	1288.7	41.7	957.5	145.6	66.8	155.1	88.8	88.8
24-T	[11]	24	0.202	189.9	12.1	0.76	724.8	35.2	1.68	1628.8	51.2	908.3	128.4	65.9	183.5	97.6	110.7
14-T	[12]	14	F	F	F	1.12	1059.7	60.3	2.34	2202.7	137.3	F	385.6	67.4	F	431.9	157.7
HPSC	[14]	22	F	F	F	0.89	844.5	45.5	2.09	1979.5	110.5	F	89.7	38.6	F	78	80.7
DPL	[15]	22	0.256	240.1	15.9	0.87	833.3	36.7	2.11	1986.3	123.7	835.6	91.9	45.6	213.9	79.9	96.2
SRCPL	[15]	20	0.193	182.8	10.2	0.7	759.8	31.1	1.79	1726	64	869.6	132.3	50.4	167.8	104.5	90.2
New-HPSC	[16]	24	0.217	205.3	11.7	0.77	739.8	30.2	2.04	1931.6	108.4	998.5	193.6	71.5	216.7	149.1	145.9
Hybrid 1	[17]	24	0.267	258.8	16.2	0.78	749.3	30.7	2.31	2176.4	133.6	932.4	189.1	60.2	248.9	145.6	139
Hybrid 2	[18]	16	F	F	F	**0.35**	**339.7**	**10.3**	**0.94**	**912.8**	**27.2**	F	231.4	69.6	F	81	65.4
Hybrid 3	[19]	22	0.169	162.6	6.4	0.68	661.1	18.9	1.53	1473.5	56.5	811.8	101.3	48.6	146.9	68.9	74.4
Hybrid 4	[20]	16	**0.113**	**106.9**	**6.1**	0.44	428.2	11.8	0.98	951.3	28.7	675.3	81.6	38.7	76.3	35.9	37.9
Hybrid 5	[21]	21	0.146	136.9	9.1	0.58	561.1	18.9	1.31	1270.4	39.6	697.5	96.8	43.9	108.1	56.1	57.5
Hybrid 6	[21]	23	0.133	125.3	7.7	0.54	522.5	17.5	1.35	1304.1	45.9	683.4	81.4	35.1	98.4	43.9	47.4
GDI D1	[22]	18	0.127	144.8	7.2	0.46	446.7	13.3	1.09	1054.7	35.3	599.8	98.8	31.8	76.17	43.5	34.7
GDI D2	[22]	22	0.165	155.6	9.4	0.63	604.6	25.4	1.49	1437.5	52.5	547.6	77.3	28.6	90.4	48.7	42.6
GDI D3	[22]	21	0.152	116.6	8.5	0.61	586.3	23.7	1.32	1277.6	42.4	708.3	90.53	39.7	114.7	55.2	52.4
Proposed	-----	22	0.129	122.2	6.8	0.48	466.6	13.4	1.17	1135.7	34.3	**523.8**	**65.7**	**25.3**	**67.6**	**31.5**	**29.6**
Performance Ratio (PR)			1.14:1	1.14:1	1.11:1	1.37:1	1.37:1	1.3:1	1.24:1	1.24:1	1.26:1	1:1.04	1:1.17	1:1.13	1:1.13	1:1.14	1:1.17

TABLE II

PERFORMANCE COMPARISON OF FULL ADDER CELLS OPERATING IN CASCADE

Supply voltage: 0.8 V, F: Failed to Operate, PR: Performance Ratio (Proposed FA Value: Best Value Obtained by Other FAs)																
Full Adder	**Ref. no**	**Power (µW)**					**Delay (ps)**					**PDP (fJ)**				
		4 bit	**8 bit**	**16 bit**	**32 bit**	**64 bit**	**4 bit**	**8 bit**	**16 bit**	**32 bit**	**64 bit**	**4 bit**	**8 bit**	**16 bit**	**32 bit**	**64 bit**
CPL	[5]	6.47	13.46	F	F	F	1256.7	4484.9	F	F	F	8.13	60.36	F	F	F
12-T	[6]	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
CCMOS	[7]	2.42	4.68	9.48	20.79	44.2	510.6	1042.5	2105.8	4233.2	8490.5	1.24	4.88	19.96	88.01	373.3
TGA	[8]	2.45	5.33	F	F	F	709.1	2145.7	F	F	F	1.74	11.44	F	F	F
TFA	[10]	2.5	4.45	F	F	F	478.7	2444.5	F	F	F	1.196	10.88	F	F	F
24-T	[11]	2.83	5.56	10.95	22.06	46.31	521.2	1078.5	2183.9	4389.6	8867.1	1.47	5.996	23.91	96.83	410.6
14-T	[12]	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
HPSC	[14]	3.24	6.3	12.45	25.98	F	561.8	1214.3	2520.2	5131.7	F	1.82	7.65	31.38	133.3	F
DPL	[15]	3.62	7.92	F	F	F	1467.6	4814.4	F	F	F	5.31	38.13	F	F	F
SRCPL	[15]	3.59	F	F	F	F	1934.3	F	F	F	F	6.94	F	F	F	F
New HPSC	[16]	2.84	5.57	11.11	22.75	F	945.5	2024.6	4203.5	8581.2	F	2.69	11.28	46.7	195.2	F
Hybrid 1	[17]	2.81	5.47	10.77	22.69	F	767.8	1552.5	3485.4	7057.8	F	2.16	8.49	37.54	160.1	F
Hybrid 2	[18]	**1.67**	**3.65**	F	F	F	1683.9	6436.7	F	F	F	2.81	23.49	F	F	F
Hybrid 3	[19]	2.53	5.41	11.69	25.45	55.94	413.3	881.6	1782.4	3572.5	7976.7	1.06	4.77	20.83	90.92	446.2
Hybrid 4	[20]	1.83	3.99	F	F	F	475.7	2487.6	F	F	F	0.87	9.93	F	F	F
Hybrid 5	[21]	2.39	5.23	F	F	F	539.6	3094.6	F	F	F	1.29	16.18	F	F	F
Hybrid 6	[21]	2.41	5.28	F	F	F	498.6	2986.3	F	F	F	1.2	15.77	F	F	F
GDI D1	[22]	1.93	4.27	F	F	F	500.3	2493.6	F	F	F	0.97	10.65	F	F	F
GDI D2	[22]	2.08	4.38	9.4	20.16	43.23	345.9	743.6	1621.2	3550.6	7985.1	0.72	3.26	15.24	71.58	345.2
GDI D3	[22]	2.57	5.56	11.86	25.94	56.87	410.7	883.1	1924.2	4290.8	9826.4	1.05	4.91	22.82	111.3	558.8
Proposed	-----	1.95	4.19	**9.01**	**19.11**	**40.19**	**285.6**	**613.8**	**1326.5**	**2946.7**	**6725.9**	**0.56**	**2.57**	**11.95**	**56.3**	**270.3**
Performance Ratio (PR)		1.17:1	1.15:1	1:1.04	1:1.05	1:1.08	1:1.21	1:1.21	1:1.22	1:1.2	1:1.19	1:1.28	1:1.27	1:1.28	1:1.27	1:1.28

To evaluate driving capability, the entire range of output loads was simulated from the fan-out of four unit-size inverters, known as FO-4, to FO-64. In this case, the supply voltage is 0.8 V. Figure 4 shows the results of the simulation. Figure 4 shows the very high AP, PDP, and latency of FO-32 and FO-64. Therefore, it has to be the best fan-out load scenario for the proposed design if it is FO-16.

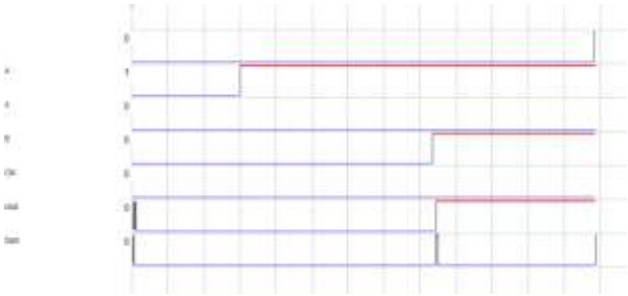

Fig 5: Simulation results for the one bit Hybrid full adder

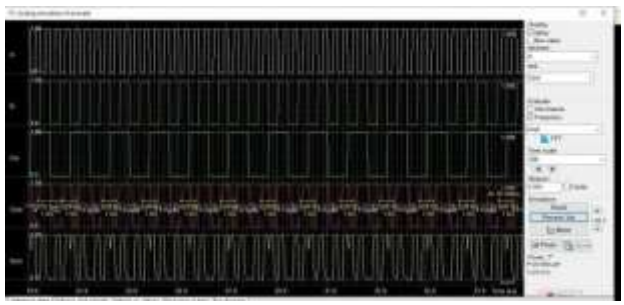

Fig 6: Analog Simulation example

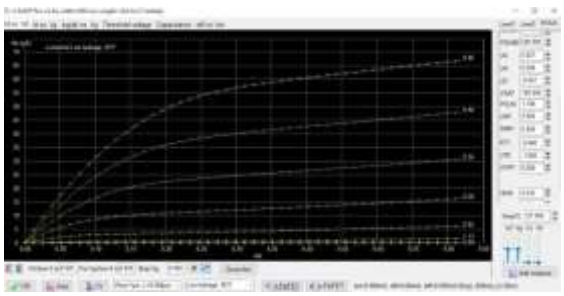

Fig 7: Simulation Layout of Hybrid Full Adder

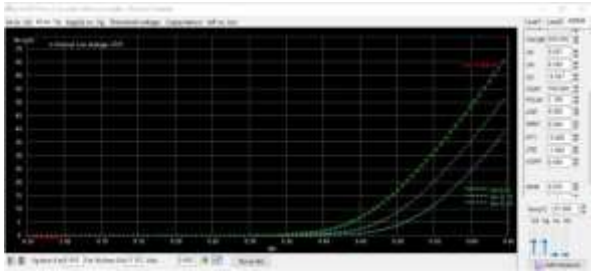

Fig 8: Ids vs Vds Characteristics

Fig 9: Ids vs Vgs Characteristics

V. Conclusion

This paper presented a hybrid full adder design optimized for 1-bit calculations that is both fast and energy efficient. The proposed architecture was evaluated using post-layout simulations, and the results demonstrated that it outperformed earlier designs in terms of delay and Power Delay Product (PDP). Simulation tests reveal that the developed FA performs better when used as a single cell in terms of PDP and speed. To demonstrate scalability, the FAs have also been extended to a 64-bit word length. On extensions up to 64-bit, only the designed FA—of which there are currently five—operates without a buffer in the interim. The performance characteristics for cascade mode indicate that the proposed architecture is slightly better for building larger wordlength adders. which happen in today's computer systems focusing both low power and high speed, compute processes.

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