

# A Novel Low- Dynamic Comparator Leveraging Cascaded Structure for Noise Minimization Power

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**Abstract—** *In this research introduces a new low-power dynamic comparator that utilizes a cascaded structure to minimize noise. The proposed comparator achieves a significant reduction in power consumption while maintaining high-speed operation. The comparator has improved noise immunity and reduced offset voltage by employing a dynamic logic approach and optimizing the cascaded structure. Simulation results have been obtained by the proposed comparator with 12.6  $\mu$ W of power consumption, 1.2 ns of propagation delay, and 1.5 mV of offset voltage. Thus, the comparator is found to be very suitable for low-power analog-to-digital converter (ADC) applications.*

**Keywords—** *Low-Power Design, Dynamic Comparator, Cascaded Structure, Noise Minimization.*

## I. INTRODUCTION

Today this emerging need for low-power, high-speed analog-to-digital converters has promoted the development of new comparators. Comparators being a critical component of the ADCs affect the entire power consumption, processing speed, and accuracy of the converters. Traditional static comparators, however, suffer from excessive power consumption, restricted speed, and are very susceptible to noise. Recently, dynamic comparators have been of considerable interest in low-power and high-speed applications. Dynamic comparators make use of a dynamic logic where the output is produced during the evaluation phase, and so the static power is minimal.

Cascoded dynamic comparator was designed to increase its noise immunity without really affecting its speed, thus making it an ideal consideration to applications where accuracy has to be power-efficient in itself. This controlled noise-holding mechanism takes into consideration the threshold voltages and transistor sizes for each cascoded stage resulting in even greater precision during adverse conditions. The new architecture marks a step forward in dynamic comparator design, promising a good solution for modern low-power but high-performing analog-to-digital conversion systems.

The cascoded dynamic comparator thus exhibits excellent noise immunity and high-speed performance, alongside improved robustness against process variations, temperature changes, and supply voltage fluctuations, which is critical in high-performance analog-to-digital conversion systems, as even minute changes can cause large errors. It is precisely in that area where this design is helpful since it promises better performance under a variety of operating conditions, making sure that the comparator remains reliable and consistent in performance over time.

## II. PROPOSED DYNAMIC DESIGN

The low-dynamic comparator designed and created is through cascaded structure that leads to maximum noise reduction power economy in the demand of high performance and low power consumption nowadays in modern electronic systems in the field of analog-to-digital conversion. The design of the cascoded double-tail architecture provides high gain and reduces noise sensitivity without compromising on the speed of response with optimum energy consumption. This cascoded configuration effectively isolates the noise sources which adds to the accuracy and reliability of this comparator. Additionally, the careful sizing of transistors in the differential amplifier (DA) and the appropriate threshold voltage tuning of the tail transistor minimizes dynamic power dissipation, thereby improving the overall energy efficiency of the comparator.

Also essential about this approach is reduced turn-on duration for the tail transistor, such that the comparator can operate even with minimum power loss. This means improvement in energy efficiency, and also in reducing the susceptibility to noise since the comparator continuously performs under different input conditions. The design of parasitic capacitances at significant positions has been perfected, thus contributing higher gain and faster switching speeds, creating even more advantages for the comparator in high-speed applications. This design goes a long way in making the proposed comparator suitable for low-power high-speed circuits, right in the middle of performance, power consumption, and noise immunity that would become crucial for future systems analog and mixed-signal.

The design aims at optimizing the sizes of the transistors in the differential amplifier (DA) and adjusting the threshold voltage of the tail transistor. This optimization decreases dynamic power dissipation and thus improves energy efficiency in a way that keeps the total speed performance of the comparator because the tail transistor is turned on for shorter duration.

Reducing the power losses during operation by a shorter switching schedule for the tail transistor results in greater overall power efficiency but without compromising speed. Incorporating further enhanced parasitic capacitance management at various critical positions gives an improvement in performance features, faster switching speeds, and gaining capability. This makes the comparator an excellent choice for high-speed analog-to-digital conversion

applications requiring high-resolution, high-speed conversion with power efficiency. This design achieves a delicate balance between low power, high speed, and noise immunity so it will be one of the best candidates for future low-power high performance in analog and mixed-signal systems. In the future, this paradigm would be useful as electronic systems become more complex so that comparators can be driven toward the future high-performance requirements of advanced systems.

### III. SIMULATION RESULTS

This comparator has been designed and implemented in the UMC 130nm CMOS process with low power for the comparator. However, the device is optimized for performance at a low supply voltage of 1.2V and consumes a minimum amount of power. This comparator can operate with a clock frequency of up to 1 GHz, so it can be used in very fast applications. This combination of low voltage and high-frequency making it an ideal balanced point of energy-saving speed meets requirements for modern electronic systems.

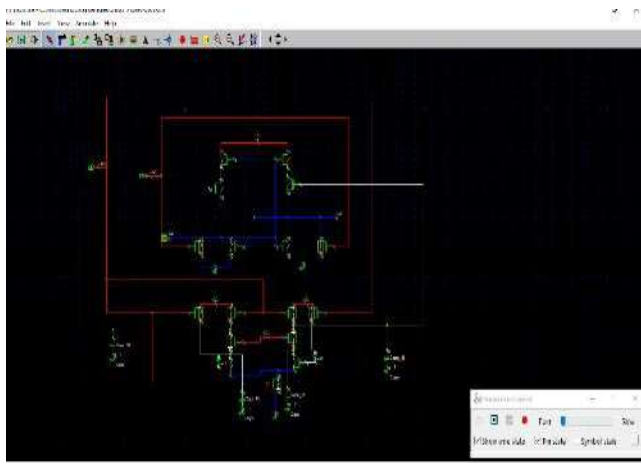


Fig1: Transient response of the proposed comparator

The process variation in source to body voltage is a factor that causes variations in the threshold voltage of NMOS of a chosen process. In this process, the maximum  $V_{thn}$  is known to appear at the minimum  $V_{SB}$ . Thus, for low power operation is selected as  $V_{DD}$ . The proposed comparator delay is determined using Monte Carlo simulations.

The given image is a circuit schematic designed using electronic design automation (EDA) software, probably for simulating or analyzing an electronic circuit. The schematic contains many components such as transistors, resistors, capacitors, and connections highlighted with colored lines, representing signal paths or power supplies. The red, blue, and white lines might indicate different signal levels, nodes, or circuit paths for debugging or simulation purposes. This kind of schematic is usually used for the design of analog or digital circuits, verification of functionality, and simulation to predict circuit behavior under different conditions. The software also includes tools such as a "Simulation Control" panel, where users can initiate simulations, view waveforms, or analyze circuit parameters like voltage and current at different nodes. Please let me know if you would like a more detailed explanation of the circuit or its parts.

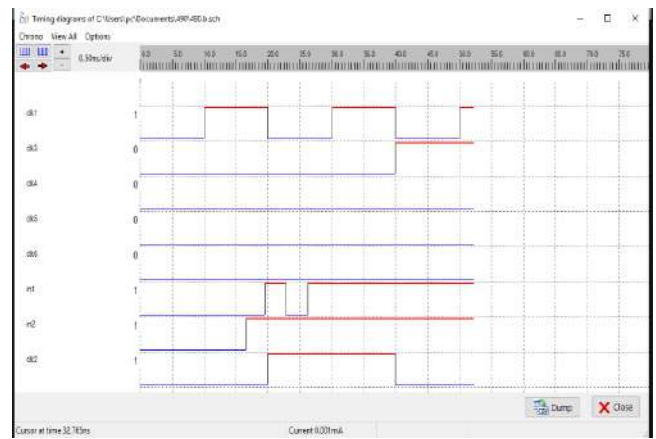


Fig2: The image given shows a timing diagram with several signal names assigned to d1, d3, d4, etc. and corresponding transitions with time.

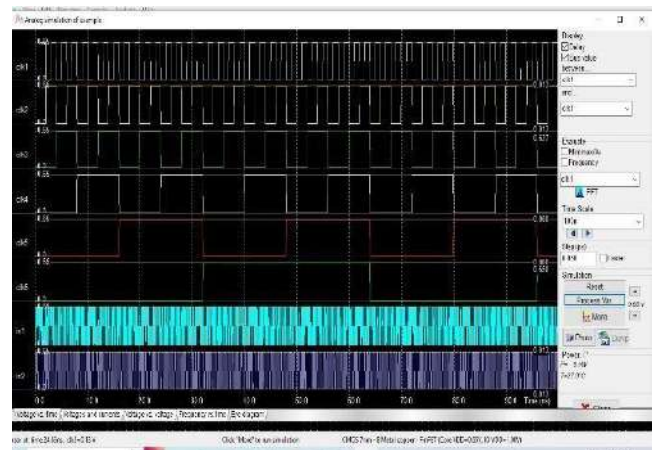
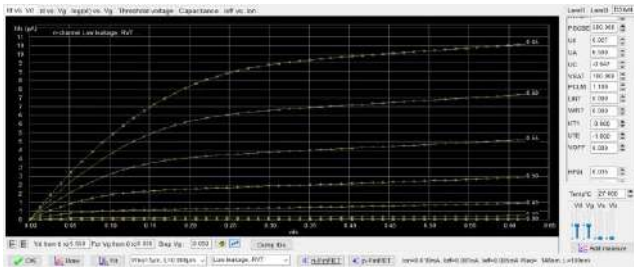


Fig3: The given image is a timing or waveform diagram that is commonly used in digital electronics to analyze and debug circuits or digital signals.

It shows several channels (ch0, ch1, etc.), each representing a signal that switches between high (logic 1) and low (logic 0) states over time. The topmost signal is a clock pulse, which is often used to synchronize operations in digital systems. Such diagrams are particularly important for understanding temporal dependencies between signals, verifying the appropriate functionality of circuits, as well as analyzing protocols in SPI, I2C, or UART. Therefore, this output most likely comes from simulation tools ModelSim, Cadence or hardware devices such as a logic analyzer or an oscilloscope. These tools serve to help engineers visualize and debug the behavior of digital systems by interpreting data transfer problems, synchronization problems, or simply timing problems in communication systems or control systems. Let me know if you want me to elaborate on any of the parts of the waveform further.



The proposed design will be able to confront such challenges by providing a considerably higher degree of stability and reliability across a wide range of conditions. The stability of the comparator can thus be maintained under process variation or changing environmental conditions over time. This type of comparator has a cascoded dynamic structure that is unique in terms of its very high-speed performance and outstanding noise immunity, which makes it suitable for the most advanced analogue to digital conversion applications. One of its most important strengths lies in its reproducibility over a wide range of common environmental and operational conditions, such as process change, temperature change, and supply voltage fluctuations. In high-speed ADC systems, even tiny deviations in these parameters can result in very large errors, which are unwelcome penalties for system performance.

This is the  $I_d$  vs  $V_{ds}$  MOSFET characteristic graph showing the operation of the device as  $V_{gs}$  changes. The curve demonstrates a linear increase in conductance and then the MOSFET has more current drain  $I_d$  for any particular value of  $V_{ds}$  when the voltage  $V_{gs}$  is increased. The curve for MOSFET demonstrates saturation, linear, and pinch-off regions.  $I_d$  becomes insensitive to  $V_{ds}$  with an almost linear dependency on  $V_{gs}$  in the saturation region. In the linear region,  $I_d$  versus  $V_{ds}$  exhibits a linear relationship, indicating the MOSFET behaves like a voltage-controlled resistor. Beyond pinch-off lies the saturation region where saturation occurs again. The important features are threshold voltage and channel length modulation with some increase in the saturation region because the effective channel length is decreased as  $V_{ds}$  increases.

#### IV. CONCLUSION

This paper presents a new latch-type comparator architecture designed for noiseless and low-power operation, as expected for submicron CMOS technologies and compact power-efficient applications. In this regard, within the preamplifier stage, a cascode structure has been designed, which effectively enhances gain while reducing input referred noise and improving the overall performance of the comparator itself. While this cascode structure provides much better noise immunity and gain, the cost for this imposes an increase in average power dissipation. The proposed design, however, uses a high threshold voltage for the tail transistor in the preamplifier, which limits the active time of the tail-transistor preamplifier taking average power to a very low level without loss of performance. Furthermore, the latch part of the

comparator is optimized very much as a low-power structure to maximize the overall energy efficiency of the circuit. This way, one can trade performance with power and energy efficiency. Thus the proposed architecture of the comparator is expected to be suitable for applications in which power consumption is critical concerned, such as portable battery-operated devices.

The dynamic comparator design uses 130 nm CMOS technology and has an input-referred noise level of 290  $\mu V$ . This low noise level makes the comparator highly suitable for analog-to-digital converters (ADCs) requiring up to 11-bit resolution, operating at a supply voltage of 1.2V. The compact design and low power consumption of the comparator make it particularly advantageous for portable and battery-powered devices, where high-resolution signal processing is essential without compromising energy efficiency. This architecture demonstrates an excellent balance between performance, noise reduction, and power efficiency, making it a strong candidate for use in high-resolution, low-power ADCs in modern electronic systems.

#### IV. REFERENCES

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