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TEST PLAN FOR REUSABLE LFSR-BASED LOW TRANSITION BIST IN 3D STACKED ICS

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Abstract
Test Scheduling is a major bottleneck in reducing the test time when it comes in the case of 3D stacked ICs since the test which has been applied in pre-bond testing may have to be applied in a different cycle in the post-bond testing due to the impending resource constraints which changes it phase. Here, a Reusable Low transition LFSR is designed which can be applied for BIST framework which be further used in case of 3D stacked ICs is proposed to schedule the tests in both pre-bond and post-bond testing accordingly. The complete framework is applied to various ISCAS-85 and 89 benchmark circuits. The BIST designs were validated at different modes of operation and the area, power overhead due to BIST is found to be negligible. From the results, it could be observed that the pseudo-Random Generator used in BIST framework is driven by Reseeded-Bit-Swapping LFSR (RBS-LFSR) which has reduced the amount of switching power dissipated from the circuit up to 25%.

1 Introduction

The emergence of 3-D stacked ICs helps us to integrate multiple silicon dies as a stack using Through Silicon Vias (TSVs) [1]. In contrast with traditional stacking the 3-D stacked designs involve less power consumption, decrease in interconnect area, decreased wire load and high percentage of stacking density. Now a days the use of 3-D Stacking, such as 3-D memory-on-processor [3], 3-D FPGA [4], 3-D NoC [2], and 3-D logic Stacks as also been predicted. VLSI chip tests can be performed in a few different types with different environments. If a new chip is designed and made before it reaches the customer, we need to ensure its accuracy design and testing process. IC testing plays an important role in ensuring that the circuit has no errors. There are many ways to test a circuit and it has also been improved over time. There are different types of testing such as verification test, production test, acceptance test etc. Test-Based IC-3-D test where several circuits are set as background and stacked one over the other through the use of Through-Silicon-Vias (TS V's) before. But because of this we get too many irregularities in the cycle which can lead to many errors and can lead to cord lengths problem. So instead, we can connect them using Controller schemes to connect the layers. When we use this type of program, we cannot use additional hardware circuitry as it may cause a larger surface area. So, we need to find a test hardware that can be built in a circuit. Among them is the BIST is another, widely used. BIST stands for Built-In-Self-Test which is used test the circuit accordingly. Computer hardware resulting from BIST additions may be empty and may be tested to a large extent to a number of times where necessary. It even reduces the cost of testing and testing time.

In VLSI Design testing plays a prominent role. The correctness of IC behaviour can be assured from the Testing phase hence it plays a crucial role. Testing in VLSI refers to testing of these designs such that they are fabricated correctly, and designed correctly. With increase in number of levels in 3D Stacked ICs the testing cost for these designs increases, hence need an architecture which can minimizes the test cost and increases the functionality. In view of these stacked designs each IC is designed with Built-in-self-Test (BIST) framework which is a design technique where a part of a circuit can be used to test the circuit by itself with minimal hardware and less cost. With the use of BIST, the same hardware can be used both in

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Prebond and Post-bond testing hence the BIST is Reusable. Pre-bond testing means to test these dies before stacking of ICs whereas Post-bond Stacking means testing of these dies after Stacking where the resource constraints come into play. The BIST framework consists of Pseudo-Random Pattern Generator, Circuit under Test (CUT), Response Analyzer and a BIST Controller to control the flow in the circuit. Among the available pattern generators used Linear Feedback Shift Register (LFSR) is most commonly used for pseudo-random pattern generation. These patterns have random numbers that are generated algorithmically through a characteristic polynomial. LFSR is a shift register whose present input is a linear function of previous state by an XOR operation between states. Linear Feedback Shift Registers are mainly of two types Standard LFSR and Modular LFSR. The Standard LFSR XOR gates feeds externally as a feedback network, which consists of D-flip-flops and exclusive –OR gates. The Modular LFSR the feedback is between adjacent flip-flops. When there is a feedback from a particular flip-flop to a flip-flop the feedback coefficient is set to one, similarly when no feedback exists it is set to zero. Compared with the standard LFSR Modular LFSR can work faster. The characteristic polynomial need to have the following properties 1) the polynomial function should be monotonic (i.e.) the higher order degree term need to be one for the switching to happen from one pattern to other pattern. 2) The characteristic polynomial should divide with $1+x^k$ where k =2n -1 which can give more number of test patterns

VLSI chip tests can be performed in a few different types with different environments. If a new chip is designed and made before it reaches the customer, we need to ensure its accuracy design and testing process. IC testing plays an important role in ensuring that the circuit has no errors. There are many ways to test a circuit and it has also been improved over time. There are different types of testing such as verification test, production test, acceptance test etc. The chip implementation has grown to sub-micron technologies integrating millions of transistors and the speed of operations has crossed rates of GHz. This has further resulted in hardware's with very high complexities. Evidently, with more levels of integration there is a possibility of more number of faults. Just when a technology matures and faults tend to decrease, a new technology based on lower sub-micron devices evolves, thereby always keeping testing issues dominant. In case of detection of faults in a traditional system it is diagnosed and repaired. However, in case of circuits, on detection of a fault the chip is binned as defective and scrapped (i.e., not repaired). In other words, in VLSI testing chips are to be binned as normal/faulty so that only fault free chips are shipped and no repairing is required for faulty ones.

Test-Based IC-3-D test where several circuits are set as background and stacked one over the other through the use of Through-Silicon-Vias (TS V's) before. But because of this we get too many irregularities in the cycle which can lead to many errors and can lead to cord lengths problem. So instead, we can connect them using Controller schemes to connect the layers. When we use this type of program, we cannot use additional hardware circuitry as it may cause a larger surface area. So, we need to find a test hardware that can be built in a circuit. Among them is the BIST is another, widely used. BIST stands for Built-In-Self-Test which is used test the circuit accordingly. Computer hardware resulting from BIST additions may be empty and may be tested to a large extent

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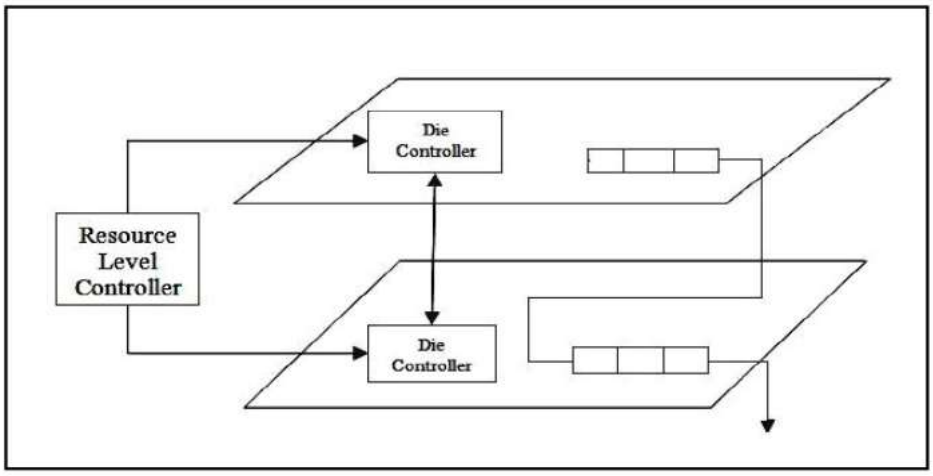

Fig1 Stacked ICs using BIST Controller

BIST is a design technique that allows a circuit to test itself. In this project the test performance achieved with the implementation of BIST is proven to be adequate to offset the disincentive of the hardware overhead produced by the additional BIST circuitry. The technique can provide shorter test time compared to an externally applied test and allows the use of low cost test equipment during all stages of production. BIST stands for Built-In-Self-Test. A BIST can have a extra hardware by which it can test the circuit by itself. It will have an BIST controller which can give command to the hardware to start its operation with a START command, Upon completion of the operation a PASS/FAIL command is given back to controller.

2 Literature survey

Faults may occur due to failure in the implementation of the design. In [1] explains the various faults that are caused during manufacturing process due to improper placement of photo resist layer. Among all other kinds of faults Stuck-at-1 and Stuck-at-0 are typical faults that need to detected and removed for the proper functioning of the chip. The prior work on 3-D Stacked ICs are based on Through Silicon Vias (TS V's) which include the analog layout structure of designing 3-D Stacks from interconnects. In [11] Xin Zhao et.al showed the way to partition the TSV using clock partitioning algorithm by reducing the wire length and clock power consumption used.In [10] B.Noia et.al proposed an new Test Access Mechanism (TAM) to transport test data on to cores, they have divide dies on to 3-types such as has, soft and firm dies to decrease the wire length used in each of the module. In [18] Rajit Karmakar et.al describes the way to test the 3-D architecture considering power and time constraints. he has defined the scheduling strategy which could schedule the constraints based on power has the radiated power need to be less for perfect functioning of the system. In [36] S. Deutsch et.al proposed an ILP model to robust the optimization which takes in to account of variations input parameter and provides an solution to reduce test time. In [28] Valentin Muregan et.proposed a way to improve test concurrency with power dissipation limits using extended tree growing algorithm by considering sequence of list and distributed-graph. In [15] Amit Kumar et.al proposed an hyper graph partition tool to connect the interconnects between the layers to reduce the wire length between them. In [8] Mukesh Agrawal et.al shows that the minimization of Wire Connect is equivalent to graph-theoretic and have proposed an technique for reuse based method at post bond testing. In [23], [22], [29] address the situation of stacking taking temperature into consideration. In [32] Yassine Fkih et.al address a problem to test the schemes before and after bonding of stacks which reduces the length of interconnects for TS Vs Stacking. In [16] Chih-Yen Lo et.al showthe architecture to connect 3-D stacks using different embedded schemes to connect the layers between them.

Linear Feedback Shift Register is a shift register whose input is an linear function of previous state. The linear function thus obtained by xor operation between states. Linear Feedback Shift Register are of mainly two types External and Internal Shift Register's In [34] E. Kalligeros et.al proposed an technique to generate

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seeds from inverting the logic value of some bits from its next state by eliminating the ROM from storing seeds which results in fast computation of seeds. In [28] R. Saraswati et.al shows a way to implement test patterns from limiting the power in the circuit by building an controller module. In [38] Dhanesh P et.al prosed an Dual Threshold Bit Swapping LFSR to reduce the transition power between vectors by considering different threshold values while swapping the bits. In [34] Nisha Haridas et.al proposed different LFSR generating polynomial that could increase the fault coverage by eliminating the total number of invalid patterns generated due to LFSR. In [35] shows the way to generate LFSR polynomials to get Maximum number of test patterns for the circuit by considering the period and shows the maximum number of primitive polynomials that has to be used to get test patterns. In [9] shows the gate level description of the different gates by converting them into sequential circuits by adding D-flip-flops.

In [23] Bogdan Dugonik et.al proposed to select the LFSR Test Pattern Generator seed to achieve highest fault coverage from given set of different characteristic polynomials. In [33] Masayuki Arai et.al proposed the application of seed selection in combination with phase shifter to evaluate the fault coverage for different circuits. In [14] J.C.Rau et.al proposed test architecture which has the advantage of both signal sharing and signal reuse properties that can minimize the xor gates and derivation time. In [32] Jiann-Chyi Rau et.al shows how to avoid generating invalid test patterns by using suggestive threshold stop point by selecting good seeds for an LFSR. In [22] shows the construction of LFSR polynomial by having multiple taps at specified spaces which could yield maximum possible test vectors for testing the circuit. In [20] A. Ahmad S. S. Al-Busaidi showed the way of getting NPP for large values of n and computing the factors for m-sequence. Built-in-Self-Test provides a special future to test the circuit by itself by providing an extra hardware circuitry and can give the fault coverage of the circuit. In [21] Y. Zorian et.al showed the process of optimization for power dissipation and diagnostic capability for identifying the failed blocks. In [26] P. Girardet.al shows the partitioning of the CUT to reduce the power utilized in the circuit. In [3] Mark G. et.al proposed a way to implement the board level self diagnostic technique by considering multiple signature analysis. In [4] Janusz Rajski et.al shows the use of scan based BIST architecture and faults developed due to the scan chain insertion. In [19] Manjunath Mosalgi et.al proposed a method to generate LFSR based pattern generator by using clock gating technique which can reduce power and can detect high fault coverage. In [16] Devika K N et.al uses an signature analysis technique by considering different signatures for testing the BIST circuit. In [11] Jamuna. S implemented a BIST Architecture used VHDL language by using signature analysis for MISR to design a BIST. In [37] P. Girard has designed an low energy BIST that cannot modify the fault coverage by analysing the selection of LFSR seed according.

Test architecture standard was motivated by the increasing device density, ball-grid-array packaging, surface mount and multiple layers, that have made the test of modern PCBs more complex and expensive by manifold. Finer pin spacing and use of double sided PCBs have limited traditional in circuit testing using bed of nails. Merging components from different suppliers required built in test delivery system that used a standard mechanism for all systems. Thus, the IEEE 1149.1 standard came into place that converted the outside nails of a bed of nails adapter into inside, electronic nails, providing access to pins without direct physical contact. It has also enabled serial read/write of test data to the core, and similar to BIST, can operate at different levels of hierarchy. The standard not only enabled components and interconnects to be tested independently, but the responses can be propagated to different components of the system from the DUT.

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3 Proposed Architecture

The proposed Reseeding Bit Swapped LFSR (RBS-LFSR) in figure.4 consists of 2 X 1 multiplexers and LFSR architecture. Consider C1, C2, C3, C4 …Cn-1, Cn be the LFSR bits where n will be the number of inputs to the CUT. When the LFSR starts switching from the initial seed it checks for the last bit Cn, it acts has a select line for all the MUX inputs. When the bit Cn is one the bits C1 and C2 are swapped simultaneously the bits C3 and C4, C5 and C6 and so on the bits are swapped with each other. The swapping of bits depends only upon the last bit Cn. With the use of this bit swapping algorithm it can account a

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percentage saving of power up to 25%. When the bit Cn is zero the swapping of bits doesn't occur and the bits remain unchanged or same.

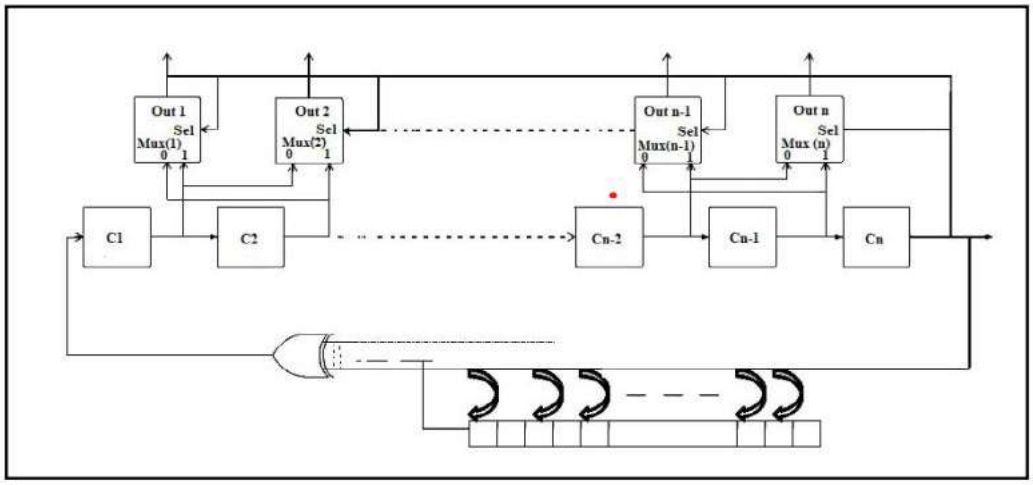

Fig 2 Reseeded Bit-Swapping LFSR.

At the same time an intermediate seed pattern is inserted during switching of these cells based on the behaviour of the circuit which can increase the amount of fault coverage to a greater extent with in limited number of test patterns. In the proposed BIST design the Test pattern Generator is designed with the use of this Reseeded Bit Swapping LFSR it can decreases the amount switching power emitted from the circuit with in limited number test patterns to satisfy the fault coverage.

Results

Here the Stacked ICs are created by stacking of two dies as shown in Table 3, and each die having three core designs. The core designs are created by using ISCAS 85, 89 benchmark circuits and two designs are created. The BIST framework for these core designs is designed. The Test pattern generators for these BIST circuits are designed using RBS-LFSR are developed and the functionality is examined over ModelSim software. The comparison of fault coverage by the use normal and RB-LFSR for a pattern count of not more than 3000 is shown in the Table 2, where the test Coverage is represented in the form of percentage. When an LFSR shifts from one pattern to another pattern it radiates some amount of switching power in the circuit by the use of RBS-LFSR the switching power can be reduced to a greater extent. The maximum clock frequencies for these benchmark circuits are calculated such that it does not violate slack times. Among the calculated frequency a desired value is chosen and kept as constant for all the circuits which are upper limits for the circuit performance. Here two parameters are used namely default toggle rate [0.02,0.08] and default probability value as [0.1,0.5] keeping these values as constant the switching power for these circuits are calculated in terms of clock cycles using Vivado tool. These values are grouped for finite set of values with finite number of clock cycles and are given as an are prescribed for Design 1, which has two dies each consisting of three cores. The values in the table represent the total number of clock cycles required to complete the test execution time. The switching power is the power radiated from the circuit when a seed shifts from one pattern to another. Table 5 shows the total amount of switching power radiated in each die in (mW) for a pattern count of 1500 and the results are compared with the use of normal LFSR and RBS-LFSR. Here the circuits used in the Die-1, Design-2 and Die-2, Design-1 have more switching activity when compared with other dies. Hence here in the last column observed that there is a total percentage decrease of about 30% when the switching power is less, the minimum amount of switching power observed is about 9% for the circuits having greater switching activity.

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Table 1: Fault Converge

	Normal-LFSR (%)	RBS- LFSR (%)
C880	98.832	98.839
C1908	96.776	98.776
C3540	95.741	97.741
C6288	98.431	99.535
S1196	96.457	97.021
S1238	91.365	91.365
S1423	96.621	97.294
S5378	96.102	96.221
S9234	65.194	87.952

Table 2 Die Design

	DIE - 1			DIE - 2		
	CORE -1	CORE -2	CORE -3	CORE -1	CORE -2	CORE -3
DESIG N-1	S1196	S1423	S5378	C880	C1908	C3540
DESIG N-2	S1238	C6288	S9234	S1423	S5378	S1238

Table 3 DESIGN 1 TESTS WITH TEST TIME IN CLOCK CYCLES AND POWER CONSUMPTIION (IN MW)

DIE 1		DIE 2	
TEST TIME	POWER (mW)	TEST TIME	POWER (mW)
100	6.635	100	11.2
250	17.74	250	28.758
200	14.389	200	23.005
300	21.391	300	34.581
150	10.739	150	17.263
350	24.99	350	40.421
400	28.53	400	42.167
450	32.218	450	30.065
300	21.494	300	8.076
200	14.321	200	5.363
100	7.253	100	2.676
250	15.523	250	6.668

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Table 4. COMPARISION OF TOTAL SWITCHING POWER FOR A PATTERN COUNT OF 1500

	Total power using Normal LFSR (mW)		Total power using RBS-LFSR (mW)		% decrease in total power	
	Die-1	Die-2	Die-1	Die-2	Die-1	Die-2
Design-1	53.022	85.99	41.72	75.64	27	13
Design-2	153.82	53.02	141.06	40.72	9.04	30

The increase in the amount of fault coverage with the use of RBS-LFSR and Normal LFSR is compared in Table 2. With the use of RBS-LFSR, can decrease the amount of switching power radiated from the circuit. The comparison between the uses of RBS-LFSR with Normal one is shown in the Table 5. There was a reduction in the amount of switching power up to 30% for smaller designs and a minimum of 9% for larger designs.

Conclusion

Here a Reusable Low transition LFSR based BIST is designed which can be stacked together to form 3D-Stacked ICs. With the help of Low Transition LFSR can decrease the amount of switching power that is radiated from the circuit, with increased amount of fault coverage. With the decreased amount of switching power in a single circuit has caused greater effect in case of Stacked IC. The components of the circuit can interact with each other and will have die and resource level controllers that can be easily programmable with bit instructions. The LFSR used is termed as Reusable, which means the same hardware can be used in pre-bond as well as in post-bond testing. To test these circuits in Stacked ICs in a particular order have modified an existing Skyline Algorithm which can schedule the tests efficiently in limited time period under Resource and Power constraints than the traditional Skyline Algorithm. With the decreased switching power a lower power constraint can be fixed instead of larger numbers. This architecture can be further extended to other bigger circuits with improved BIST designs.

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