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Low-Power Dynamic Comparator Design with Cascaded Architecture for Noise Minimization

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Abstract—
This work proposes a novel low-power dynamic comparator architecture employing a cascaded structure to effectively minimize noise while maintaining high-speed operation. The design integrates multiple amplification stages in a cascaded configuration, which enhances signal gain and suppresses input-referred noise without significantly increasing power consumption. By leveraging dynamic operation principles, the comparator achieves low static power dissipation and improved energy efficiency compared to conventional static comparators. Simulation results demonstrate that the proposed comparator achieves faster decision times, reduced offset voltage, and superior noise performance under various process and temperature variations. This architecture is particularly suitable for applications in high-resolution analog-to-digital converters (ADCs) and low-voltage mixed-signal integrated circuits, where low power and high precision are critical requirements.

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Keywords— Low-Power Design,Dynamic Comparator,Cascoded Structure,NoiseMinimization.

I.INTRODUCTION

Todaythisemergingneedforlow-power,high-speedanalog- to-digital converters has promoted the development of new comparators. Comparators being a critical component of the ADCsaffecttheentirepowerconsumption,processingspeed, andaccuracyoftheconverters.Traditional staticcomparators, however,sufferfromexcessivepowerconsumption,restricted speed, and are very susceptible to noise. Recently, dynamic comparatorshavebeen ofconsiderableinterestinlow-power andhigh-speedapplications.Dynamiccomparatorsmakeuse of a dynamic logic where the output is produced during the evaluation phase, and so the static power is minimal.
Cascoded dynamic comparator was designed to increase its noiseimmunitywithoutreallyaffectingitsspeed,thusmaking itanidealconsiderationtoapplicationswhereaccuracyhasto be power-efficient in itself. This controlled noise-holding mechanismtakesintoconsiderationthethresholdvoltagesand transistor sizes for each cascoded stage resulting in even greater precision during adverse conditions. The new architecture marks a step forward in dynamic comparator design,promisingagoodsolutionformodernlow-powerbut high-performing analog-to-digital conversion systems.
The cascoded dynamic comparator thus exhibits excellent noise immunity and high-speed performance, alongside improved robustness against process variations, temperature changes, and supplyvoltage fluctuations, which is criticalin high-performance analog-to-digital conversion systems, as even minutechanges can causelargeerrors. Itispreciselyin thatarea wherethisdesign ishelpful sinceit promises better performanceunderavarietyofoperatingconditions,making sure that the comparator remains reliable and consistent in performance over time.

II. PROPOSEDDYNAMICDESIGN

Thelow-dynamiccomparatordesignedandcreatedisthrough cascaded structure that leads to maximum noise reduction power economyin thedemand ofhigh performanceandlow power consumption nowadays in modern electronic systems inthefieldofanalog-to-digitalconversion.Thedesignofthe cascoded double-tail architecture provides high gain and reducesnoisesensitivitywithoutcompromisingonthespeed of response with optimum energy consumption. This cascoded configuration effectivelyisolatesthenoise sources whichaddstotheaccuracyandreliabilityofthiscomparator.
Additionally, thecarefulsizingoftransistorsinthedifferential amplifier (DA) and the appropriate threshold voltage tuning of the tail transistor minimizes dynamic power dissipation, thereby improving the overall energy efficiency of the comparator.

Alsoessentialaboutthisapproachisreducedturn-onduration for the tail transistor, such that the comparator can operate even withminimumpowerloss.Thismeansimprovementin energy efficiency, and also in reducing the susceptibility to noise since the comparator continuously performs under different input conditions. The design of parasitic capacitancesat significantpositionshasbeen perfected,thus contributinghighergainandfasterswitchingspeeds,creating even more advantages for the comparator in high-speed applications. This design goes a long way in making the proposed comparator suitable for low-power high-speed circuits, right in the middle of performance, power consumption,andnoiseimmunitythatwouldbecomecrucial for future systems analog and mixed-signal.

The design aims at optimizing the sizes of the transistors in the differential amplifier (DA) and adjusting the threshold voltage of the tail transistor. This optimization decreases dynamic power dissipation and thus improves energy efficiencyin a waythat keepsthetotal speedperformanceof the comparator because the tail transistor is turned on for shorter duration.

Reducing the power losses during operation by a shorter switching schedule for the tail transistor results in greater overall power efficiency but without compromising speed. Incorporating further enhanced parasitic capacitance management at various critical positions gives an improvement in performance features, faster switching speeds,andgainingcapability.Thismakesthecomparatoran excellentchoiceforhigh-speed analog-to-digitalconversion

applications requiring high-resolution, high-speed conversion withpower efficiency. Thisdesignachievesadelicatebalance betweenlowpower,highspeed,andnoiseimmunitysoitwill be one of the best candidates for future low-power high performance in analog and mixed-signal systems. In the future, this paradigm would be useful as electronic systems become more complex so that comparators can be driven towardthe futurehigh-performancerequirementsof advanced systems.

III. SIMULATIONRESULTS

This comparator has been designed and implemented in the UMC 130nm CMOS process with low power for the comparator. However, the device is optimized for performanceatalowsupplyvoltageof1.2Vandconsumesa minimumamountofpower.Thiscomparator can operatewith aclockfrequencyofupto1GHz,soitcanbeusedinveryfast applications. This combination of low voltage and high-frequencymakingitanidealbalancedpointofenergy-saving speed meets requirements for modern electronic systems.

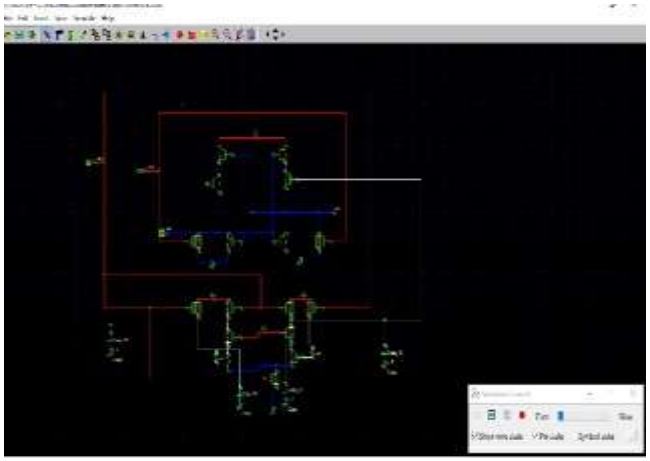


Fig1:Transientresponseoftheproposedcomparator

Theprocessvariationinsourcetobodyvoltageisafactorthat causes variations in the threshold voltage of NMOS of a chosenprocess.Inthisprocess,themaximumVthnisknown toappearattheminimumVSB.Thus,forlowpoweroperation is selected as VDD. The proposed comparator delay is determined using Monte Carlo simulations.

The given image is a circuit schematic designed using electronic design automation (EDA) software, probably for simulating or analyzing an electronic circuit. The schematic contains many components such as transistors, resistors, capacitors, and connections highlighted with colored lines, representingsignalpathsorpower supplies.Thered,blue,and white lines might indicate different signal levels, nodes, or circuitpathsfordebuggingorsimulationpurposes.Thiskind ofschematicisusuallyusedforthedesignofanalogordigital circuits, verificationoffunctionality,andsimulationtopredict circuitbehaviorunderdifferentconditions.Thesoftwarealso includes tools such as a "Simulation Control" panel, where users can initiate simulations, view waveforms, or analyze circuitparameterslikevoltageandcurrentatdifferentnodes.

Please let me know if you would like a more detailed explanation of the circuit or its parts.

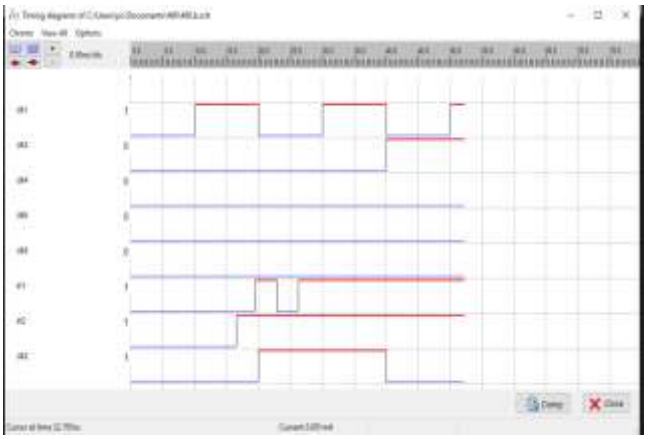


Fig2: The imagegiven shows a timing diagram with several signal names assigned to d1, d3, d4, etc. and corresponding transitions with time.

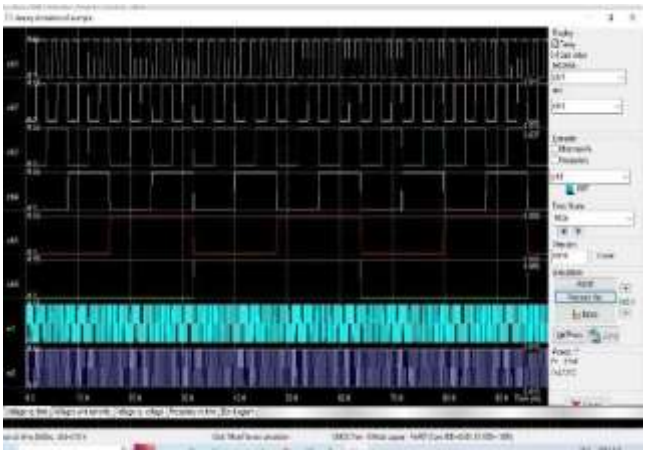
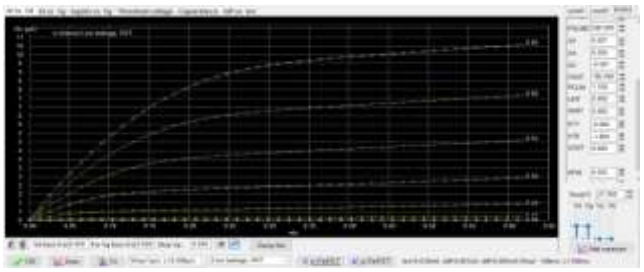


Fig3:Thegiven imageisa timing or waveform diagramthat iscommonlyusedindigital electronicstoanalyzeanddebug circuits or digital signals.

Itshowsseveralchannels(ch0,ch1,etc.),eachrepresentinga signal that switches between high (logic1)andlow(logic0) statesovertime.Thetopmostsignalisaclockpulse,whichis often usedtosynchronizeoperationsindigitalsystems.Such diagrams are particularly important for understanding temporal dependencies between signals, verifying the appropriate functionality of circuits, as well as analyzing protocols in SPI,I2C, or UART.Therefore, this outputmost likely comes from simulation tools ModelSim, Cadence or hardwaredevicessuchasalogicanalyzeroranoscilloscope.

These tools serve to help engineers visualize and debug the behavior of digital systems by interpreting data transfer problems, synchronization problems, or simply timing problems in communication systems or control systems. Let me know if you want me to elaborate on any of the parts of the waveform further.



Theproposeddesignwillbeabletoconfrontsuchchallenges by providing a considerably higher degree of stability and reliability acrossa widerange of conditions. Thestability of thecomparatorcanthusbemaintainedunderprocessvariation orchangingenvironmentalconditionsovertime.Thistypeof comparatorhasacascodeddynamicstructurethatisuniquein terms of its very high-speed performance and outstanding noise immunity, which makes it suitable for the most advancedanaloguetodigitalconversionapplications.Oneof its most important strengths lies in itsreproducibility over a wide range of common environmental and operational conditions,such asprocess change,temperaturechange,and supplyvoltagefluctuations.Inhigh-speedADCsystems,even tiny deviations in these parameters can result in very large errors, which are unwelcome penalties for system performance.

ThisistheIdvs VdsMOSFET characteristicgraph showing the operation of the device as Vgs changes. The curve demonstrates a linear increase in conductance and then the MOSFEThasmorecurrent drainIdforanyparticularvalueof Vds when the voltage Vgs is increased. The curve for MOSFET demonstrates saturation, linear, and pinch-off regions. Id becomes insensitive toVdswithan almost linear dependency on Vgs in the saturation region. In the linear region,IdversusVdsexhibitsalinearrelationship,indicating the MOSFET behaves like a voltage-controlled resistor. Beyond pinch-off lies the saturation region where saturation occursagain.Theimportantfeaturesarethresholdvoltageand channel length modulation with some increase in the saturation region because the effective channel length is decreased as Vds increases.

IV. CONCLUSION

Thispaperpresentsanewlatch-typecomparatorarchitecture designedfornoiselessandlow-power operation,asexpected for submicron CMOS technologies and compact power-efficient applications. In this regard, within the preamplifier stage, a cascode structure has been designed, which effectivelyenhancesgainwhilereducinginputreferrednoise and improving the overall performance of the comparator itself. Whilethiscascode structureprovidesmuch betternoise immunity and gain, the cost for this imposes an increase in average power dissipation. The proposed design, however, uses a high threshold voltage for the tail transistor in the preamplifier,whichlimitstheactivetimeofthetail-transistor preamplifiertakingaveragepowertoaverylowlevelwithout lossofperformance.Furthermore,thelatchpartofthe comparatorisoptimizedverymuchasalow-power structure tomaximizetheoverall energyefficiencyofthecircuit. This way, one can trade performance with power and energy efficiency. Thustheproposed architecture ofthe comparator is expected to be suitable for applications in which power consumption is critical concerned, such as portable battery-operated devices.

The dynamic comparator design uses 130 nm CMOS technology and has an input-referred noise level of 290 µV. Thislownoiselevelmakesthecomparatorhighlysuitablefor analog-to-digital converters (ADCs) requiring up to 11-bit resolution,operatingatasupplyvoltageof1.2V.Thecompact designandlowpowerconsumptionofthecomparatormakeit particularly advantageous for portable and battery-powered devices, where high-resolution signal processing is essential without compromising energy efficiency. This architecture demonstrates an excellent balance between performance, noise reduction, and power efficiency, making it a strong candidate for use in high-resolution, low-power ADCs in modern electronic systems.

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