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Design and Implementation of a Fin FET-Based Hybrid Full Adder Using GDI in 18nm CMOS

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Abstract— This hybrid logic Full Adder circuit is designed using Modern applications, ranging from consumer electronics to large-scale computing systems, require circuits that are faster, smaller, and more energy-efficient. Whether it is low-power IoT devices, mobile processors, or AI hardware, every

NOR logic gates and implemented by FINFET transistors. For the design, GDI of CMOS 18nm technology has been used. The simulation and testing for MICROWIND program are utilized to evaluate the load-pulling capabilities of the circuit.

HFA's hybrid logic design minimizes latency and consequently also reduces the power consumption as compared with the traditional adder circuits. These characteristics ensure that this proposed design is very suitable for high-speed applications as well as energy-efficient applications. NOR logic gates are used to design the hybrid logic Full Adder circuit, and FINFET transistors are implemented inside it.

The circuit is simulated, along with the testing of pull loads using the MICROWIND tool. It adopts CMOS technology with a scale of 18nm CMOS in GDI (Gate Diffusion Input) technique. HFA uses hybrid logic with the design having lower latency and low power dissipation compared to the traditional design of the adders. for the above architecture may be used for high-speed applications as well as for energy-efficient ones.

Keywords— **NOR Logic Gates, FINFET Transistors, CMOS 18nm Technology, Gate Diffusion Input (GDI), Low Power Consumption, High-Speed Applications, Energy-Efficient Circuits, Load-Pulling Simulation, MICROWIND Tool, Digital Circuit Design, Low Latency, Powe6r Dissipation**

1. INTRODUCTION (HEADING1)

Electronics have made dramatic changes in the life of a modern human being. The main change is said to have taken place mainly in the field of microprocessors, communication devices, and dsp which involves digital circuits.

It hastened the development of the development of battery-operated portable electronics, such as computers, tablets, mobile-phones, and notebooks. Therefore, to improve the life span of these gadgets while reducing energy consumption, manufacturers have made the two main criteria to work around them.

Modern applications, ranging from consumer electronics to large-scale computing systems, require circuits that are faster, smaller, and more energy-efficient. Whether it is low-power IoT devices, mobile processors, or AI hardware, every improvement in circuit design can make a significant difference in terms of performance and power consumption. As Moore's Law continues to push the limits of transistor miniaturization, the need for innovative circuit design techniques becomes more apparent. This is where Gate Diffusion Input (GDI) emerges as a transformative solution for developing optimized circuits. The Limitations of Conventional Design Techniques.

2. The Limitations of Conventional Design Techniques

Power Consumption: The greatest problem of the modern circuits is about power-efficiency. The traditional CMOS that has large dynamicandstaticpower that tendsto dissipated thus limiting it s application which restricts their use in energy.

3. Olden Design Techniques:

1. CMOS (complementary metal oxide semiconductor) logic:
Advantages: Strong operation, noise immunity, and scalability.
Disadvantages: Higher transistor count, larger area, and higher power consumption.

2. PASS TRANSMISSION LOGIC(PTL):

Advantages: Lower transistor count than CMOS, better area efficiency.
Weaknesses: Signal degradation due to voltage drops, poor noise margins, and design complexity.

3. Transmission Gate LOGIC (TGL)

Strengths: Improved logic flexibility and reduced power consumption.
Weaknesses: Higher transistor required for complex circuits.

GDI-invention:

GDI methodology as we have seen that there are disadvantages achieved by when we design the digital

circuits using other methodologies to overcome these disadvantages we are designing circuits using GDI.

Advantages:

1. GDI minimizes the transistor count and power consumption while maintaining CMOS compatibility.
2. GDI provides similar area benefits as PTL but avoids the voltage degradation issues by maintaining proper voltage swing.

Applications of GDI in Circuit Design

1. Arithmetic Circuits:
GDI is applied to design adders, multipliers, and other arithmetic units since it is low-power and high-speed.

2. Combinational Logic:
Basic gates, multiplexers, and complex combinational functions can be implemented using GDI in a very efficient manner.

3. Sequential Circuits: Flip-flops, registers and counters that are implemented
with GDI have lesser power consumption along with reduce d area when compared with the traditional implementation.

4. Low-Power Applications: GDI circuits are also suitable for portable devices, medical electronics, and IoT sensors, which require energy efficiency

5. High-Performance Systems: Processors and Data processing units can be applied with GDI to deliver improved switching performance and longer times

Hybrid Full Adder (HFA):

The full adder hybrid type is the digital circuit that combines the complementary metal-oxide-semiconductor logic, the pass-transistor logic, and transmission gates with the full adder circuit and thus it maximizes the performance. It is characterized as a hybrid because it uses all the technologies to which it belongs to exploit advantages in either, or all, or only some of those factors: Power consumption, Delay, Area, Power-Delay-product.

FINFET Based Hybrid Full Adder:
FINFET-based hybrid adder is a type of digital circuit designed to perform binary addition using hybrid architectures that integrate the advantages of multiple adder topologies, implemented using **FINFET (Fin Field Effect Transistor)** technology.

This is a mixture of conventional CMOS for robustness and GDI to reduce the transistor count and increase efficiency.

Energy-Efficiency:

GDI reduces dynamic power dissipation to a great extent to reduce the switching activity. Low leakage current, due to having fewer transistors compared to the pure CMOS.

Power Dissipation:

In certain settings, GDI loses some short-circuit power but offers superior control over power dissipation.

Trade-off:
The transistor configuration is no-longer standard and neither is the layout complexity. It means that the GDI methodology compromises signal inte grity and noise margin.

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Error-Distance:

It is due to hybridization of CMOS for the correct operations Error distance is relatively small but can be enhanced considerably with high-frequency operation and low supply voltage.

Methodology:

The Gate Diffusion Input (GDI) methodology is a design technique used primarily in digital integrated circuits, especially for low-power and high-performance applications. GDI minimizes power consumption and area by simplifying the logic gate implementations compared to traditional CMOS logic Gate.

The GDI approach uses very few transistors; often, two or three transistors are used in one logic gate. The method offers much greater freedom in the design of complex gates and is therefore much better suited for modern applications that require dense and efficient logic circuits. Together with advanced topologies such as simplified mirror adders and below is a detailed break- up of the Gate Diffusion Input methodology, its principles and how it is applied:.

GDI logic is a very simple and very powerful concept where three inputs are applied per transistor rather than the normal two used in the case of CMOS design. Inputs of the GDI cell include: the gate(G), source(P), and the drain (N).

The GDI method maintains the fundamental benefits of CMOS technology but works on the weaknesses of this technology with respect to power, area, and speed.

Gate-Diffusion-Input (GDI) is a novel logic design methodology that focuses on low-power, high-speed circuits in terms of reduced-power consumption.

This is very effective for digital integrated-circuit- design, such as arithmetic circuits, in which both Area and power efficiency are crucial.

Simplified Design: The traditional logic gate structure is replaced with GDI gates, which comprise a simplified configuration of transistors that only uses two transistors per logic gate, whereas traditional CMOS designs use 3-4 transistors.

Low Power Consumption: GDI gates also result in low power consumption. Diffusion terminals share between logic gates, meaning the capacitive load reduces, as does switching-loss.

High-Speed:
The low number of transistors and low capacitance helps in crease the circuit speed.

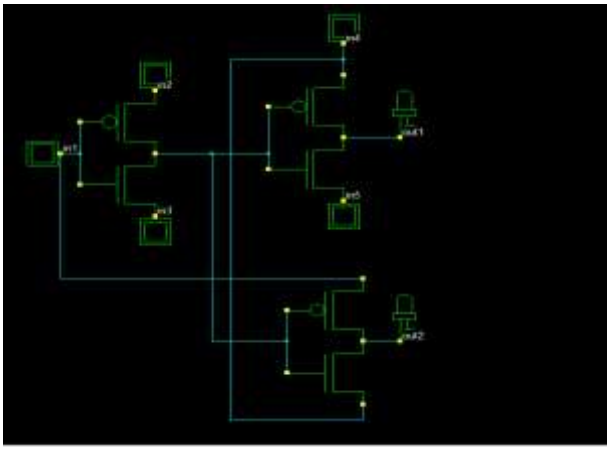

Fig1: Conventional CMOS full adder design using GDI

This circuit is a hybrid of CMOS logic and GDI methodology. This GDI decreases the number of transistors used in a design compared to the CMOS. It combines the PMOS and NMOS for effective signal processing. The circuit is designed using Conventional CMOS its input is nor gate and output is and gate.

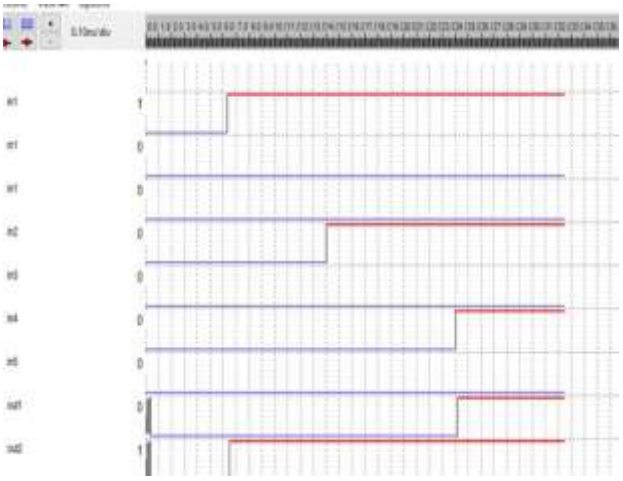

Fig2: Timing Diagram of Conventional CMOS full adder design in GDI methodology

Table 1: Design of Conventional CMOS full adder design in GDI

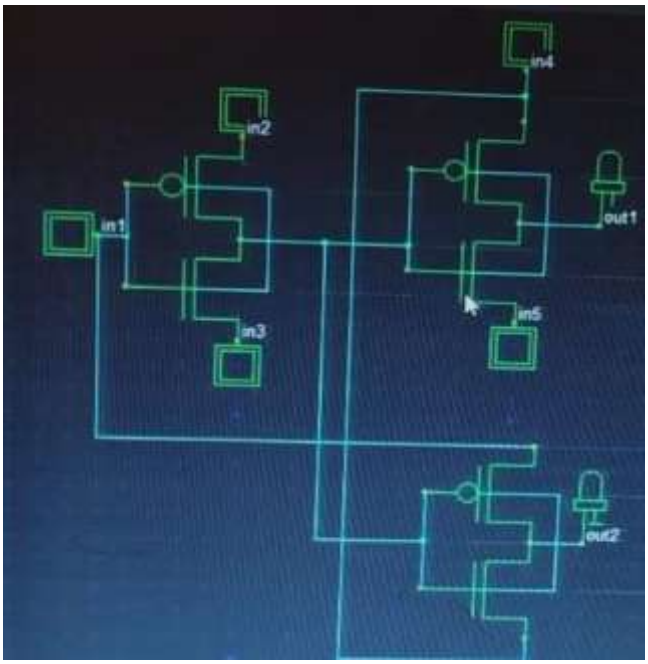

Fig3: FINFET based full adder design in GDI using NOR gate

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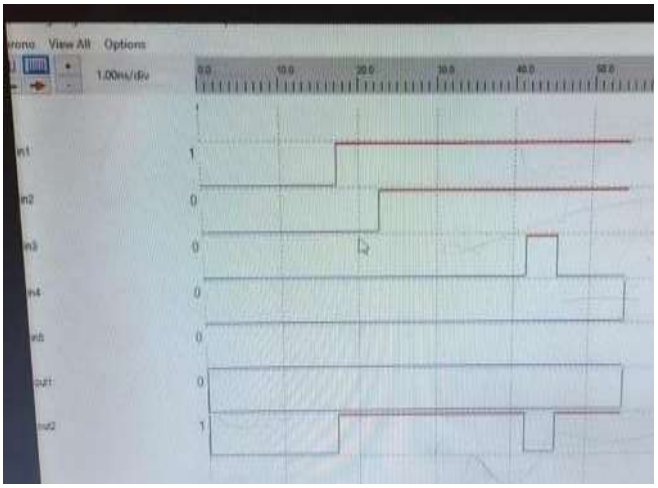

Fig4: FINFET based full adder design in GDI using NOR gate

Conclusion:

The FINFET-based GDI full adder design demonstrates better performance characteristics (lower power, delay, and leakage) compared to the **conventional CMOS GDI design**. This makes it a more viable choice for advanced applications in low-power, high-speed digital systems, especially in deep-submicron and nanoscale technologies. This paper is designed for the FA topologies of power optimization.

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